PRR-HEC-Elec-C6

Experience with the MPI-96B Chip of the GaAs Front-End System for the ATLAS HEC

– Milestone Document –

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1 Introduction

The baseline choice for the amplifier front-end electronics of the hadronic end-cap calorimeter (HEC) of ATLAS is based on the concept of "active pads"[1, 2]. The signals from two consecutive pads are fed into a separate preamplifier which is located close by at the circumference of the calorimeter wheel inside of the liquid argon. The amplified signals of a certain number (4, 8 or 16) of double pads in subsequent readout planes are actively summed at the same location. These summed signals form the longitudinal readout structure which is read out via cold to warm feedthroughs.

The concept was developed and successfully tested in the framework of the RD33 experiment[3]. In 1996 the prototype calorimeters of the HEC have been equipped with monolithic GaAs amplifier chips of RD33. In a second round of tests, the prototype calorimeters were equipped with the first prototype GaAs chip (MPI-95)[4] of the HEC architecture. These prototype calorimeters have been exposed to testbeams at CERN. The results of these

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tests have been presented to the LARG community, they are summarized in a forthcoming LARG note[5].

The chip MPI-95 was thoroughly reviewed by the Milano group of D.Camin. Results and recommendations were presented to the LARG community.

A milestone document was presented by the MPI HEC group to the LARG community[6]. On the basis of the results and recommendations, the LARG community decided in fall 1996 to go ahead with the cold GaAs front-end for the HEC module-0 as the baseline solution. A milestone was introduced to be met with the chip series of the module-0. It is defined as (see minutes of LARG Group Representative Meeting 8.11.1996): **"The most critical Milestones are :**

- **a noise figure (at 2 nF) better or equal to what 0T would do (240 nAmp at 40 ns peaking to triangle)**
- **less or equal than 3 summing amp dead after two cool downs and HV run (there are 140 such amps for mod 0).Less than 4dead after the same two cool downs."**

In 1996, two different GaAs prototype chips have been developed (MPI-96A and MPI-96B) taking into account the recommendations by the Milano group. A comparison between the two designs was made on the basis of two batches of 200 such chips. The chip MPI-96B (sometimes also called BB96B after the designers J.Ban and H.Brettel) was chosen for the module-0 calorimeters. A total of 806 chips were received and submitted to the qualification tests developed for the final series[20].

We present here a summary of results which are described in detail in separate notes[11]-[22]. They contain a.o. the results of the measurements of the performance of the GaAs chip, of their radiation hardness, of their high voltage safety, and of the regime of formation of bubbles on the housing of the chip.

This document is aimed at the milestone set for the GaAs front-end of the HEC module-0 in order to proceed to the series production.

2 Requirements

The environment in which the electronic front-end has to be operated is characterized by high pile-up rates and relatively high radiation levels. A neutron fluence of $\sim 2 \times 10^{13}\, n\, cm^{-2}$ and a photonic dose of 100 krad are typically accumulated over a period of ten years. The operation of a large number of amplifier channels in the liquid argon puts an upper limit on the power consumption of <30 mW/channel.

From the point of view of jet energy resolution[7], an appropriate parameter range of the electronics requests a gain equality of the preamplifier channels which enter into one summing channel of $< 5\%$, a maximum of the nonlinearity in both the high and the low signal range of 3%, an accuracy of the calibration system of better than 1%, and a timing accuracy of better than 2 ns.

The lower end of the signal range is defined by the signal of minimum ionizing particles (MIP) which should be detectable for physics purposes. It is 88 MeV for a readout cell of 2 double gaps and 352 (704, 1408) MeV for a readout channel in the first (second, third) longitudinal section. The maximal energy is determined for the reference 5 TeV jets. The maximum expected in any one of the readout cells along the 40 planes of the HEC is observed around the gaps 6 to 8 from the front. It is ~8000 times higher than the energy deposited by a MIP in a readout cell. In the summed readout sections either 8 or 16 gaps are grouped into one channel. The maximum energy of 1940 GeV (2780) for one readout channel in the first (second) longitudinal section is ~5500 times higher than the MIP signal in an 8-/16-fold section. Consequently, a readout system of 14-bits is needed.

3 Noise Performance

In Fig. 1 the electronic noise of the chip MPI-96B is shown as function of detector capacity as measured in liquid nitrogene.

Figure 2 shows a comparison of the electronic noise of the chip MPI-96B as measured at room temperature and in LN2 for a peaking time of 40 ns.

The distribution of the electronic noise from mass measurements of the chip MPI-96B at room temperature for a shaping time of 50 ns is displayed in Fig. 3.

In Fig. 4 the distribution of the electronic noise measured on one PSB board equipped with chips MPI-96B is given for measurements at room temperature (left) and in LN2 (right) for two working voltages V_{ee}=-2.0 V (top) and -2.5 V (bottom).

Figure 5 shows the distribution of the mean electronic noise per readout channels as observed in testbeam measurements with the rear prototype calorimeter equipped with the MPI-95 chip.

The noise distribution for three readout channels as observed in testbeam measurements with the rear prototype calorimeter equipped with the MPI-95 chip is displayed in Fig. 6.

Using above information, the resulting contribution of the electronic noise in the various η regions of the HEC as derived from characteristic noise measurements of chips MPI-96B in LN2 in the lab. for peaking times of 40 ns in the region $1.5 < \eta < 2.5$ and 30 ns for larger η is obtained as given in Fig. 7. The contribution of the electronic noise is displayed for the three longitudinal section separately.

4 Reliability Test

Figure 8 shows the response of 160 ADC channels to pulses of 500 DAC counts at a reference measurement during the second LAr filling. Only 138 channels were connected in this setup. One channel was dead at the time of installation of the calorimeters, a second one was weak. The unconnected channels and the dead and weak channels are marked in the figure.

In Fig. 9 the gain of channels with four preamplifiers at the input as function of detector capacity as determined by calibration measurement during the second LAr filling. In a similar manner Fig. 10 displays the gain of channels with eight preamplifiers at the input and Fig. 11 the gain of channels with sixteen preamplifiers at the input.

A comparison of amplitude measurements for all preamplifier channels of ten PSB boards before and after two cooling cycles in the HEC cryostat is shown in Fig. 12. It is observed that all of the 1096 preamplifiers are still alive and give rather similar results as before the installation on the calorimeter modules. In a similar way one recognizes that all of the 138 read-out channels which were alive at the beginning of the installation yield the same result as before except one which weakened. It turned out that a capcitor at the input to one of the preamps died. As a consequence of this failure a slight redesign of the PSB board is made introducing a blocking capacitor at the input of the driver stage.

In conlusion we remark that none of the GaAs chips failed.

5 Next Steps

The following steps are foreseen towards the series production of the HEC front-end electronics:

- Declaration of the LARG community that the milestone of module-0 has been met.
- Declaration of production readiness by ATLAS following the production readiness review (PRR) of Dec.8th, 1997.
- Placement of the complete order for the GaAs chips.
- Production of a dedicated mask set.
- Production of all GaAs wafers in one technology run.
- DC die sort and selection of good wafers.
- Special DC tests on wafer as agreed upon between MPI and the producer.
- Cutting of wafers.

- Assembly of 1/3 of chips, delivery in July 1998. The second 1/3 to be delivered in April 1999, the third 1/3 in January 2000.
- All chips will be submitted to the stringent quality control procedures as defined in the QA plan[20].
- In parallel the radiation hardness of the series production will be probed with sufficient statistics. These tests will be done in Dubna.
- In parallel the PSB boards will be ordered and delivered according to a similar time schedule.
- The fully equipped PSB boards will be submitted to the stringent quality control procedures as defined in the QA plan[20].
- The PSB boards will be sent to CERN where they will be mounted on the calorimeter modules as these arrive from the assembly sites for final cold tests in the HEC cryostat at CERN.

6 Conclusion

It has been demonstrated that the goals of the milestone have been met:

- The noise level measured with the new GaAs chip MPI-96B for a detector capacity of 2 nF is 150 nA including cables, i.e. well below the noise level of 240 nA defined a year ago for this milestone.
- All 1036 preamplifier channels and all 138 read-out channels robustly survived the harsh surroundings of the two cooling cycles in the HEC cryostat.

The performance characteristics of the preamplifiers fulfills the requirements[12, 16, 20].

Extensive tests have demonstrated the hardness of the electronics against radiation levels as expected for the envisaged surroundings in the HEC; a safety factor of at least 10 is clearly visible[19].

For the specific electrode structure of the HEC with HRC coating the amplifiers have proven to be robust against high voltage discharge both under harsh test conditions and in 'real life' during the testbeam of the prototype in the most disfavourable orientation (upside down)[18].

Specifically designed investigations of bubble formation have been carried out both on the housing of single GaAs chips in a special setup and on fully equipped PSB boards in the HEC cryostat simulating the final ATLAS conditions. These investigations as well as accompanying flow calculations have provided the insight that no bubbles will be formed under the pressure and temperature conditions in the ATLAS cryostats. For the most unfavourable position at the bottom of the cryostat a safety margin of at least a factor of four is observed[21, 22].

We therefore ask the LARG community to declare that the milestone has been met and that the series production may start.

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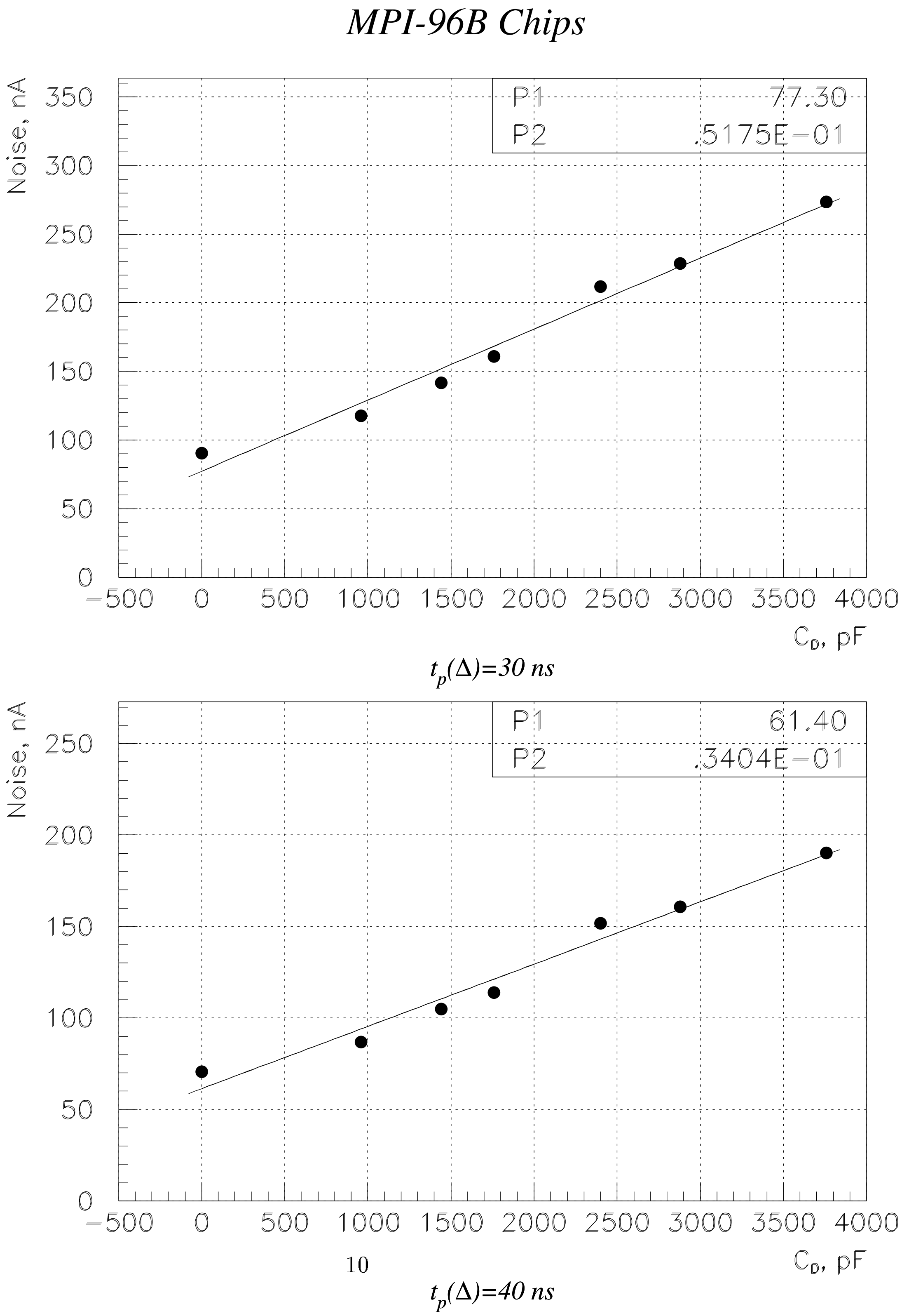


Figure 1: Electronic noise versus detector capacity for the chip MPI-96B for two different peaking times.

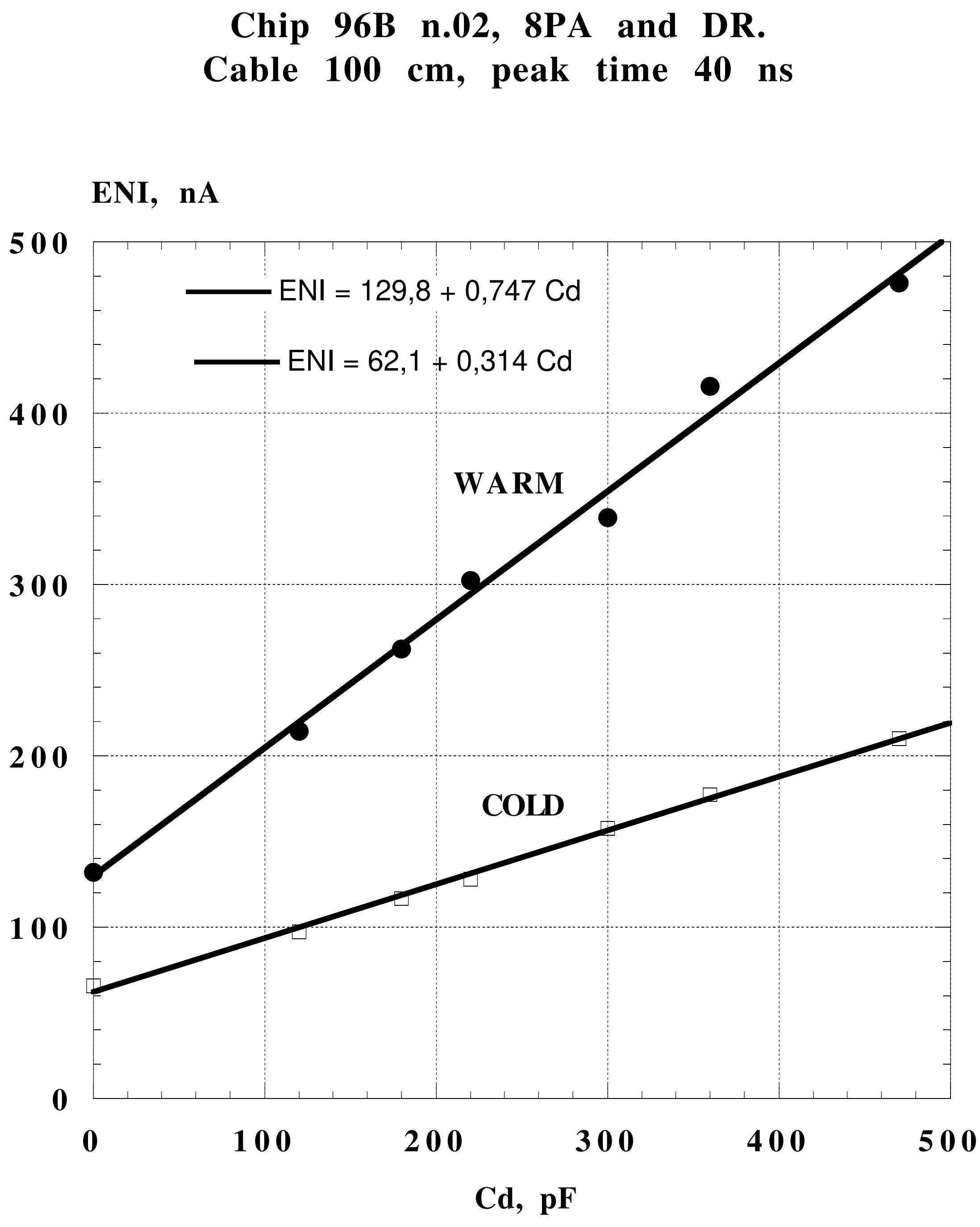
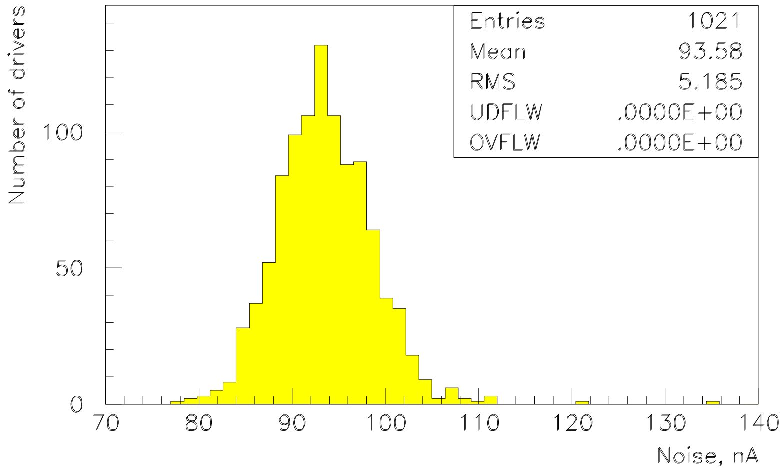
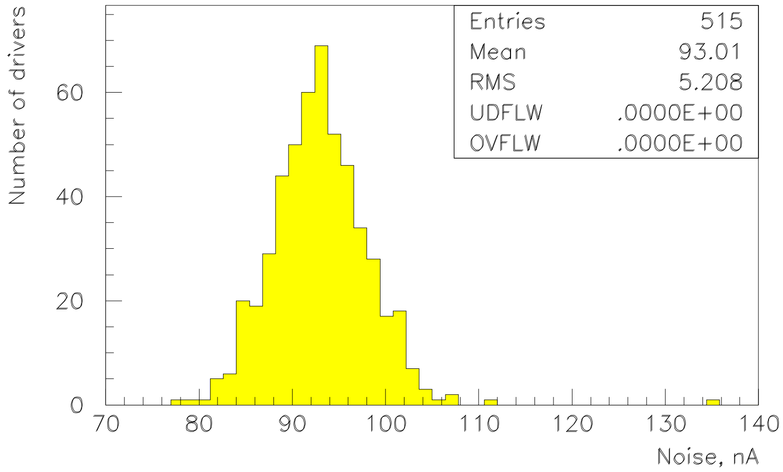


Figure 2: Comparison of the electronic noise of the chip MPI-96B as measured at room temperature and in LN2 for a peaking time of 40 ns.

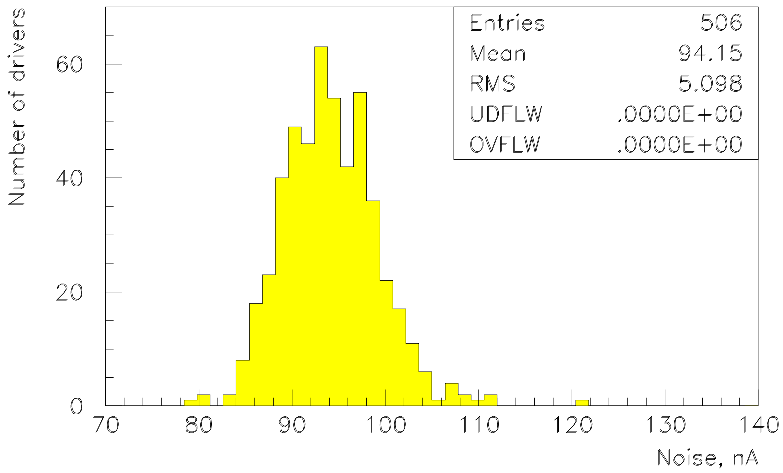
Set of Chips 2: Equivalent Noise in Measurement 1



All drivers



Drivers no.1



Drivers no.2

Figure 3: Distribution of the electronic noise from mass measurements of the chip MPI-96B at room temperature for a shaping time of 50 ns.

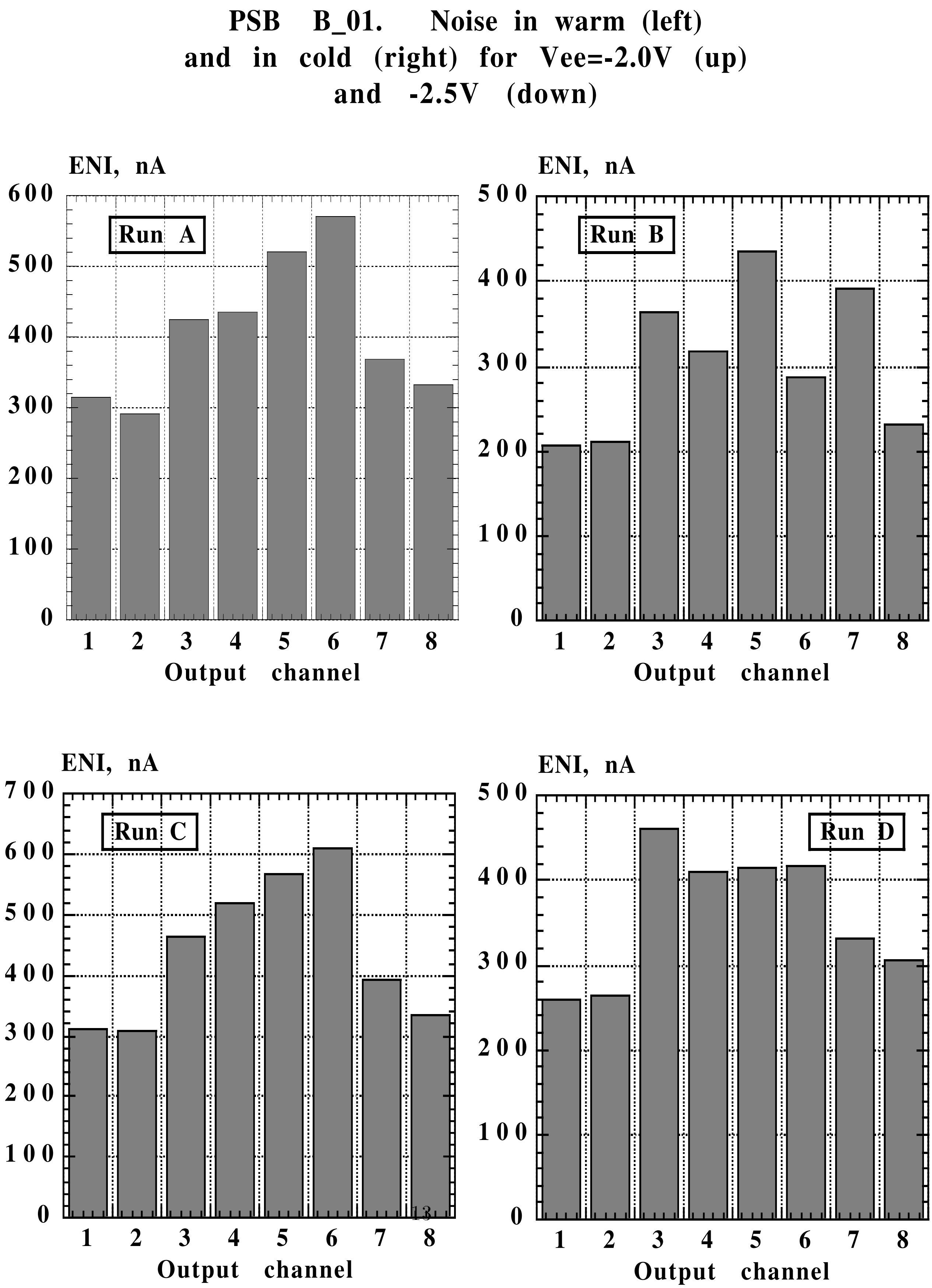


Figure 4: Distribution of the electronic noise at room temperature (left) and in LN2 (right) from measurements of one PSB board equipped with chips MPI-96B for two working voltages V_{ee}=-2.0 V (top) and -2.5 V (bottom).

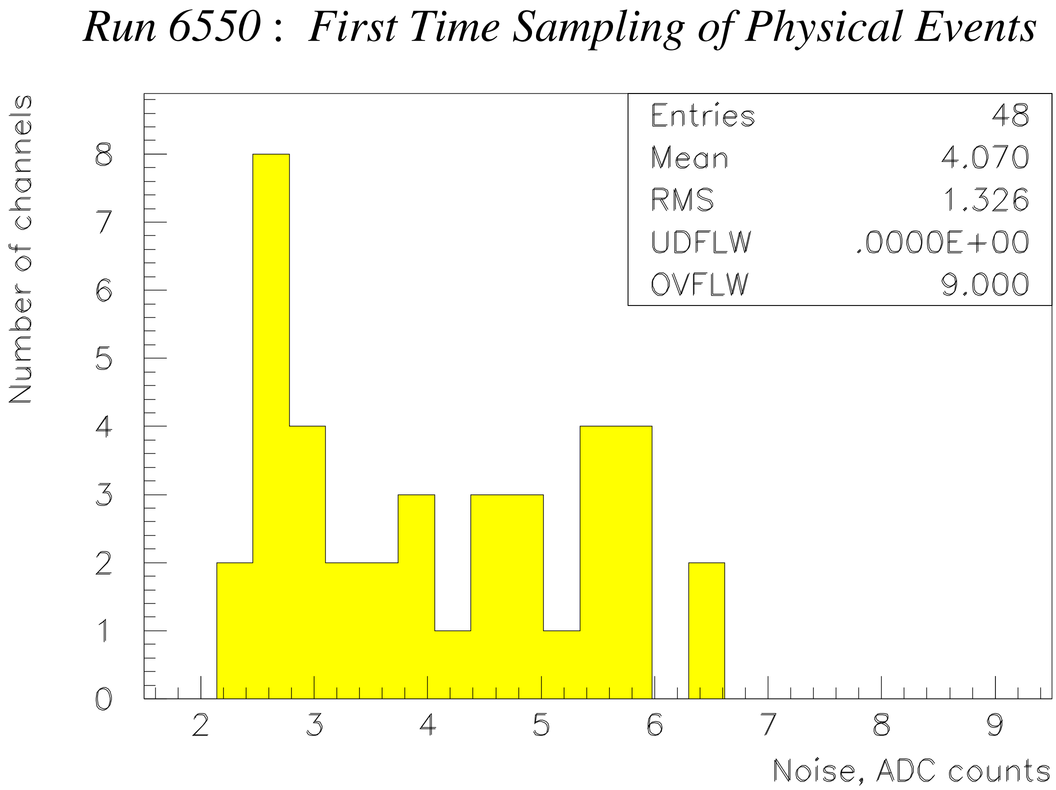


Figure 5: Distribution of the mean electronic noise per readout channels as observed in testbeam measurements with the rear prototype calorimeter equipped with the MPI-95 chip.

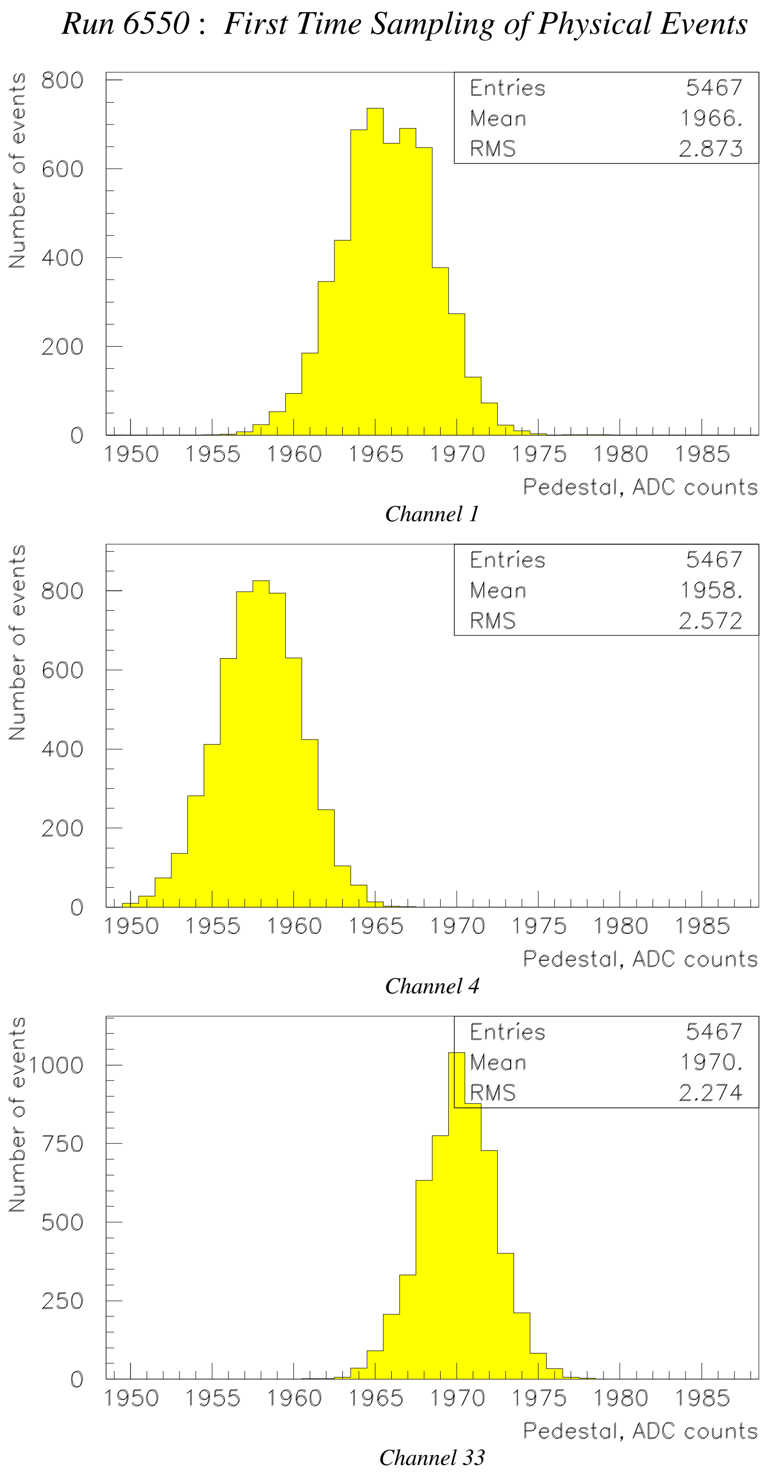


Figure 6: Noise distribution for three readout channels as observed in test-beam measurements with the rear prototype calorimeter equipped with the MPI-95 chip.

Electronic Noise in the HEC

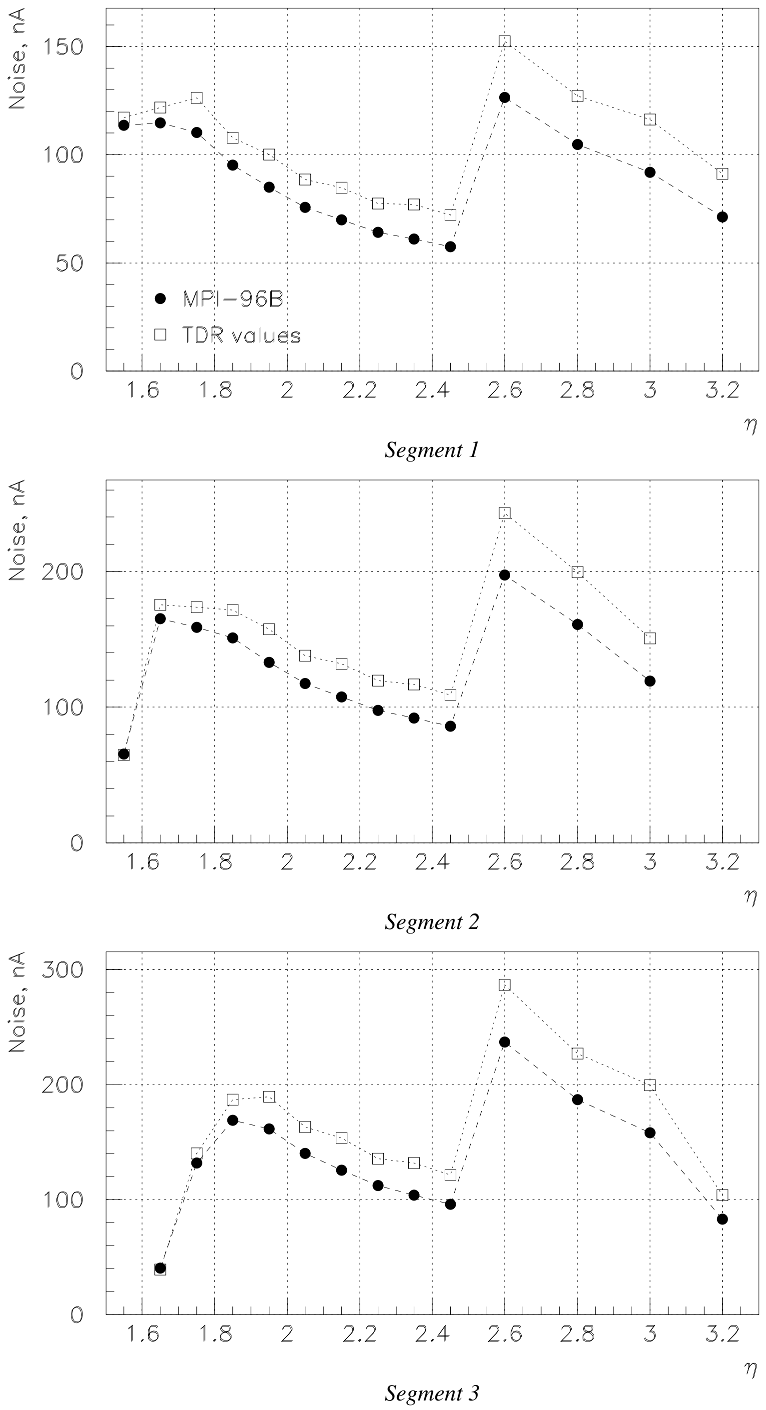


Figure 7: Contribution of the electronic noise in the various η regions and for three longitudinal segments of the HEC as derived from characteristic noise measurements of chips MPI-96B in LN2 in the lab. for peaking times of 40 ns in the region $1.5 < \eta < 2.5$ and 30 ns for larger η.

Figure 8: Response of 160 ADC channels to pulses of 500 DAC counts at a reference measurement during the second LAr filling.

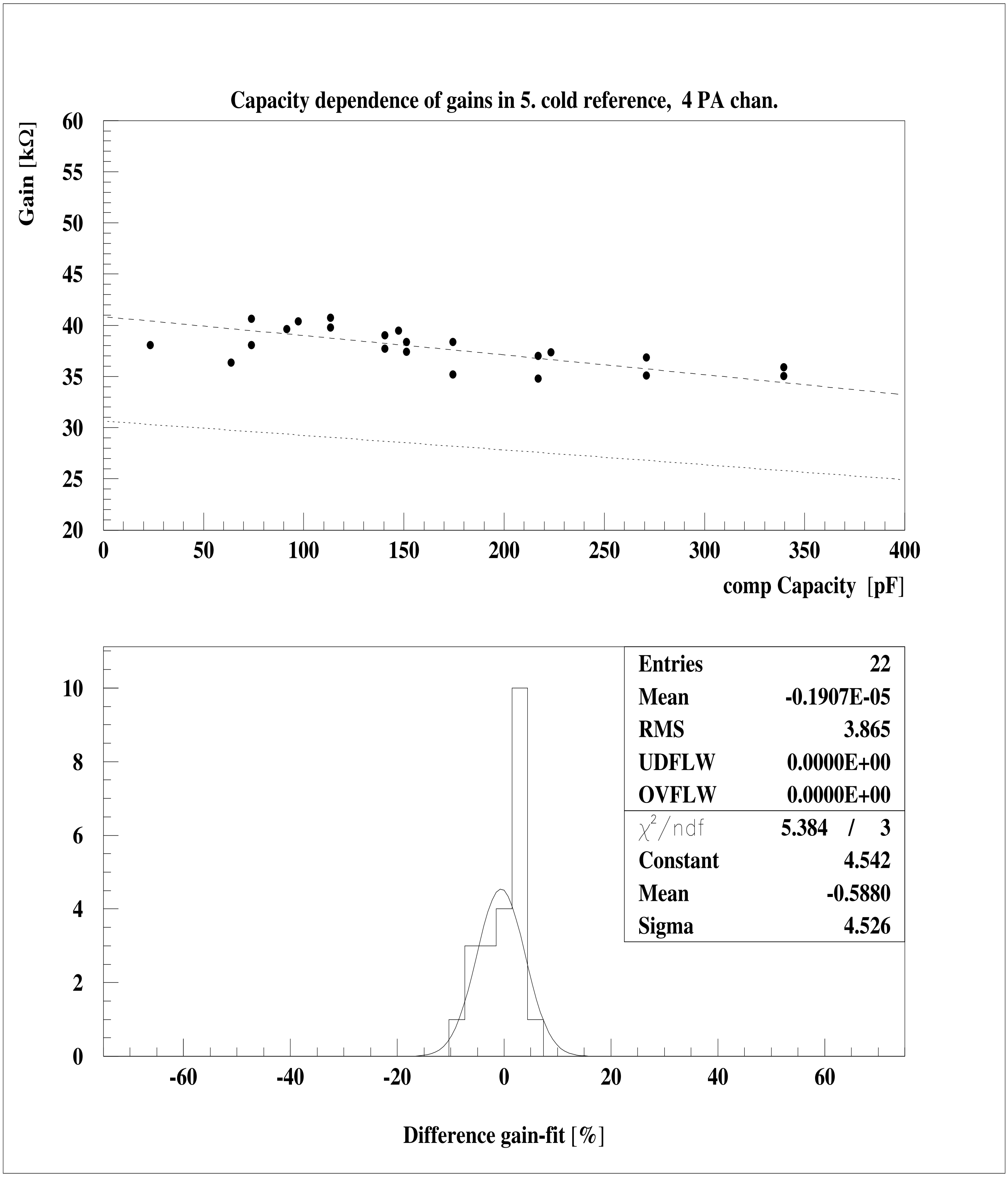


Figure 9: Gain of channels with four preamplifiers at the input as function of detector capacity as determined by calibration measurement during the second LAr filling.

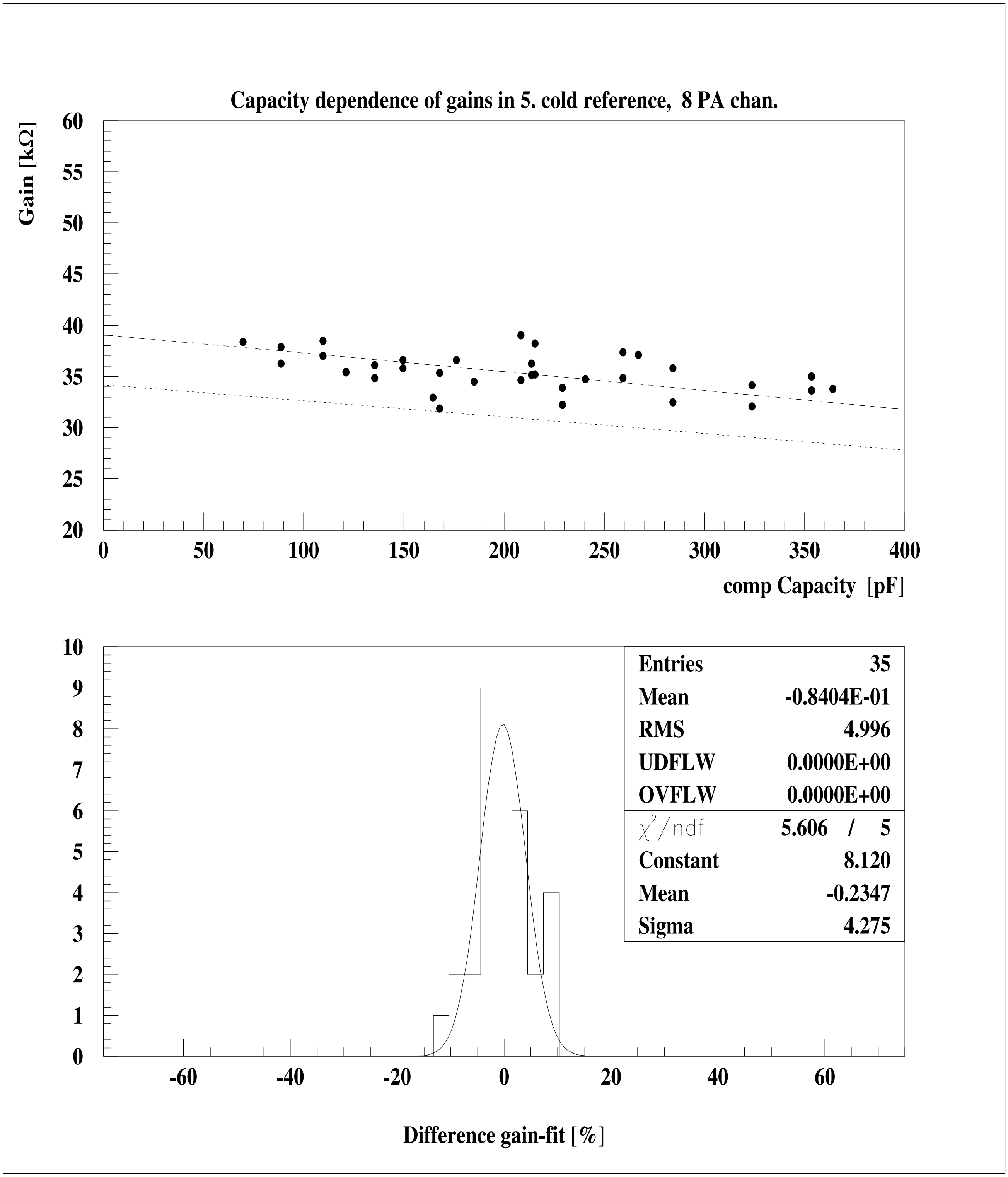


Figure 10: Gain of channels with eight preamplifiers at the input as function of detector capacity as determined by calibration measurement during the second LAr filling.

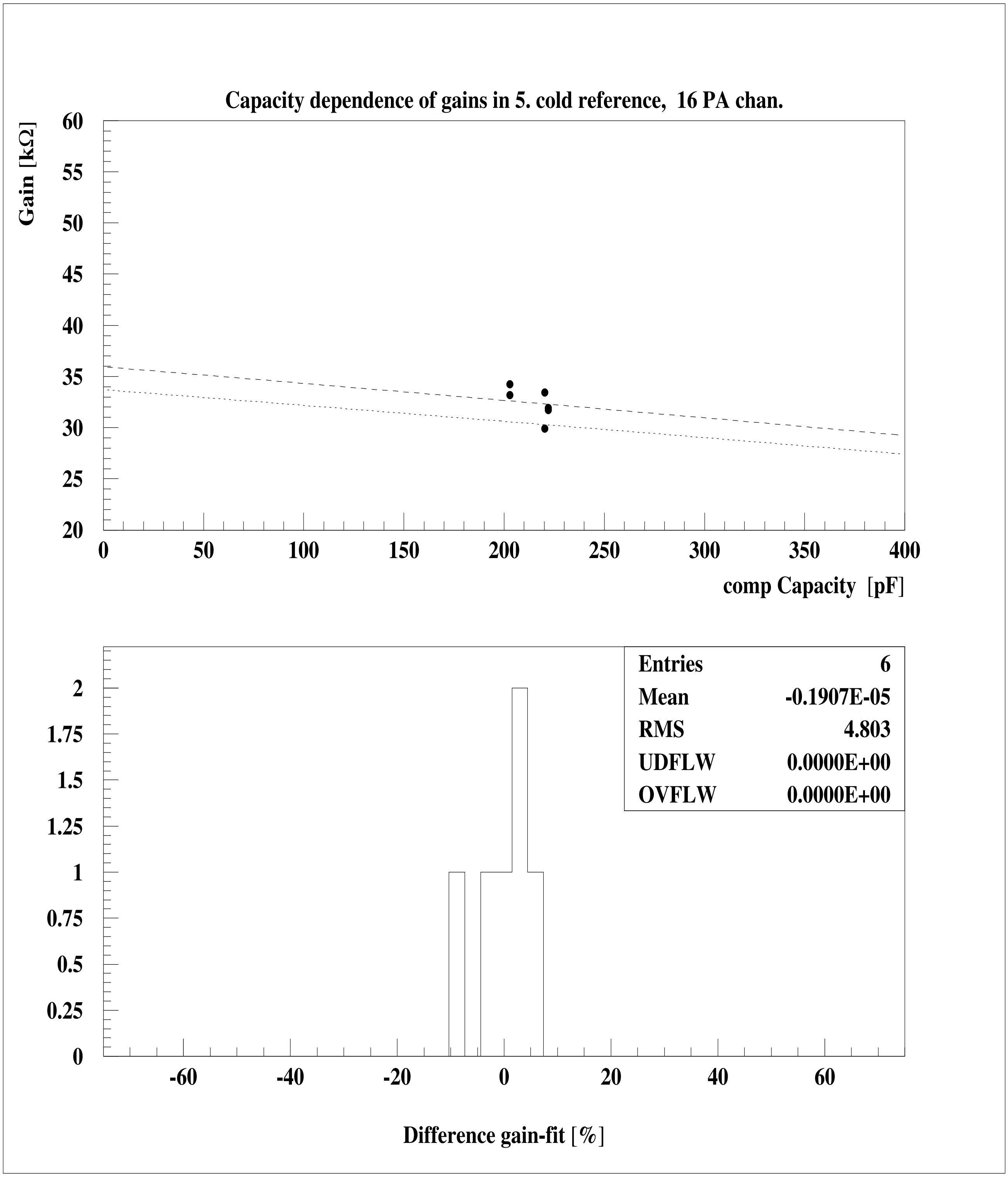


Figure 11: Gain of channels with sixteen preamplifiers at the input as function of detector capacity as determined by calibration measurement during the second LAr filling.

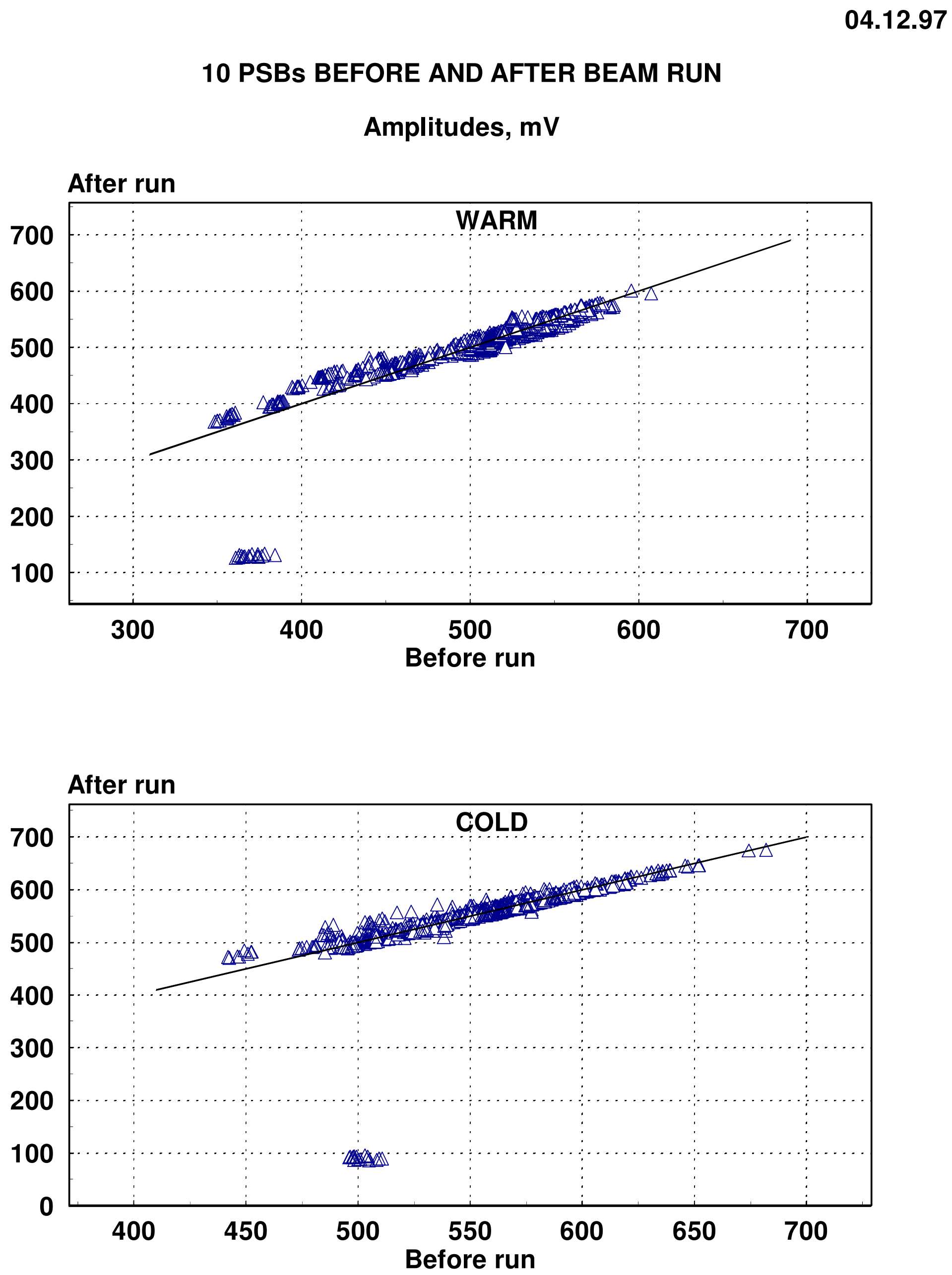


Figure 12: Comparison of amplitude measurements for all preamplifier channels of ten PSB boards before and after two cooling cycles in the HEC cryostat.