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Tower Driver Board for the ATLAS Hadronic End-Cap and Forward Calorimeters

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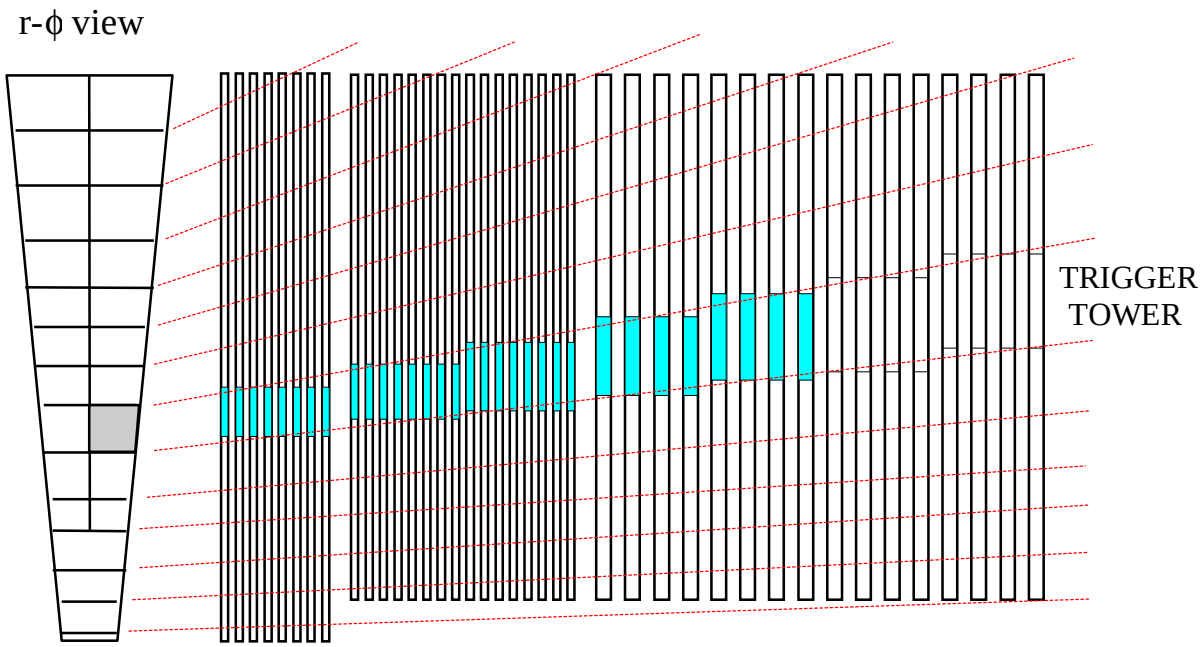
Abstract. This Note presents documentation for the Design Review of the tower driver board. The HEC trigger towers pattern and signals summing scheme are described. The board specification requirements, design and results of the SPICE simulations are presented. The prototype (1/3 of full board) have been produced and tested in laboratory conditions and in the HEC test beam environment. The full-size board has also been designed, produced and tested. The results of these tests are presented. Finally, the plans of the further developments and measurements as well as production schedule are discussed.

Table of Contents

1. Introduction

1.1 HEC readout and trigger towers

One wheel of the hadronic end-cap calorimeter (HEC) consists of 32 ϕ-wedges, each of them have 24 η,ϕ bins and 4 longitudinal readout segments, shown schematically on Fig.1. The size of bins is $\eta x \phi$=0.1x0.1 for $\eta < 2.5$ and 0.2x0.2 for high η So, each wedge has 96 readout cells, 8 of them are empty because of the first low-η bins are not present in the longitudinal segments 3 and 4, and the last high-η bin is not present in segments 2 and 3. The readout channel is formed by analog summation of signals from individual gaps in preamplifying and summing boards, situated on the outer side of the wedge.



GAPS	1-8	9-16	17-24	25-28	29-32	33-36	37-40
BLOCKS	1	2	3	4	5	6	7
SEGMENTS	1	2		3		4	

Figure 1: *Segmentation of HEC wedge in r-, ϕ- and z- directions*

The trigger tower is formed by analog sum of signals from 4 longitudinal segments of the same η,ϕ location. This summing is performed by the Linear Mixer (LM) of the shaper chip [1] in the front-end boards (FEB). In contrary to the case of electro-magnetic calorimeters, no further summation of signals is needed for the L1 trigger system. That is why a special type of Layer Sum Boards (LSB) are used for the HEC channels [2]. The board, which finally builds trigger towers of the HEC is called Tower Driver Board (TDB) since no summation is implied there. The function of this board is to produce differential signals and to drive 70-m trigger cables.

Simulations of the high-energy jets in ATLAS show that the energy deposition in the HEC last longitudinal segment is very low, typically a few % of total energy deposition. In this case the signal to noise ratio is better if to exclude the 4-th segment from the trigger sum. This can be done by the proper programming of the FEB, therefore it does not affect the TDB design.

In the case of the forward calorimeter, the trigger towers are formed by two steps of summing in LM and in LSB. Since no further summation is needed, the TDB will be used also for this detector.

1.2 Readout and trigger channels in one HEC quadrant

The η-bins of the HEC wheel are numbered from 2 to 15 as shown on Fig.2. In the low η-region there are 16 ϕ-bins (A to P) and in the high-η region there are 8 ϕ-bins (A to H). One HEC quadrant (8 wedges) is read out by 6 FEBs placed in one front-end crate [3]. The cable connections are made in such a way that one FEB processes an η-region of 4 ϕ-wedges. Hereafter we number these FEBs from 1 to 6 according to Fig.2. Each FEB delivers 32 trigger signals, so in total there are 192 trigger channels per quadrant. These signals are collected to two TDB, so each board has 96 channels. We number these TDB as 1 and 2 as shown on Fig.2.

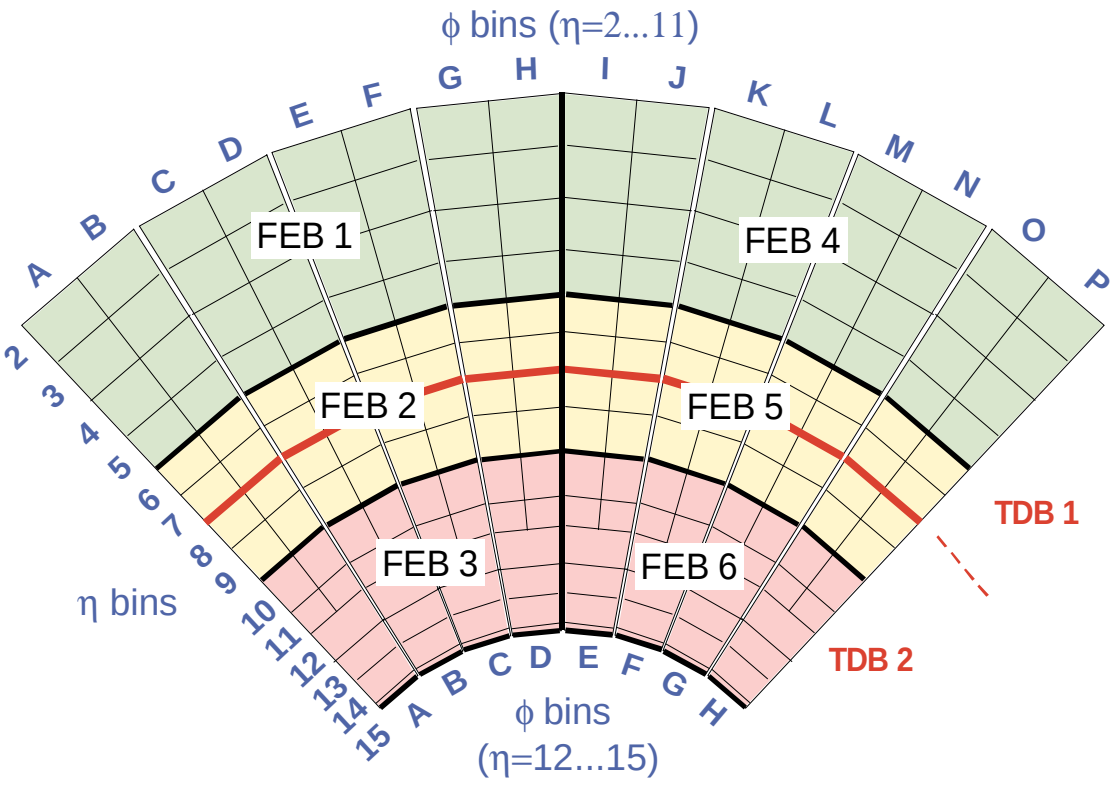


***Figure 2**: η,ϕ regions of the HEC quadrant and corresponding FEB and TDB numbering.*

The numbering of the readout channels is organized according to the FEB's numbering scheme. The channels of the first half-quadrant (FEB 1...3) are numbered from 1 to 384 and in the

second half (FEB 4...6) – from 385 to 768. The second part has a structure, equivalent to the first part. The first 4 channels of FEB1 are connected to 4 longitudinal cells of tower A2, the next 4 channels – to tower B2, then C2, D2, A3, B3, and so on. The first 64 FEB channels deal with ϕ-bins A...D and η-bins 2...5, the last 64 channels – with ϕ-bins E...H and the same η-bins. So, the numbering of readout channels has natural periodical structure with groups of 64 channels, presented in Tab.1.

Table1: *Numbering of readout channels in the HEC half-quadrant.*

Readout channels	1...64	65...128	129...192	193...256	257...320	321...384
HEC towers	A2...D5	E2...H5	A6...D9	E6...H9	A10...B15	E10...D15
FEB	FEB 1		FEB 2		FEB 3	

1.3 Trigger signals amplitudes and timing

The amplification factors of trigger channels have to be chosen from the condition that amplitudes for E_T = 256 GeV are between 1500 and 3000 mV. Fig.3 shows the TDB input amplitudes calculated for E_T = 256 GeV. The gains of LM and of LSB are selected to minimize the spread between different η-bins.

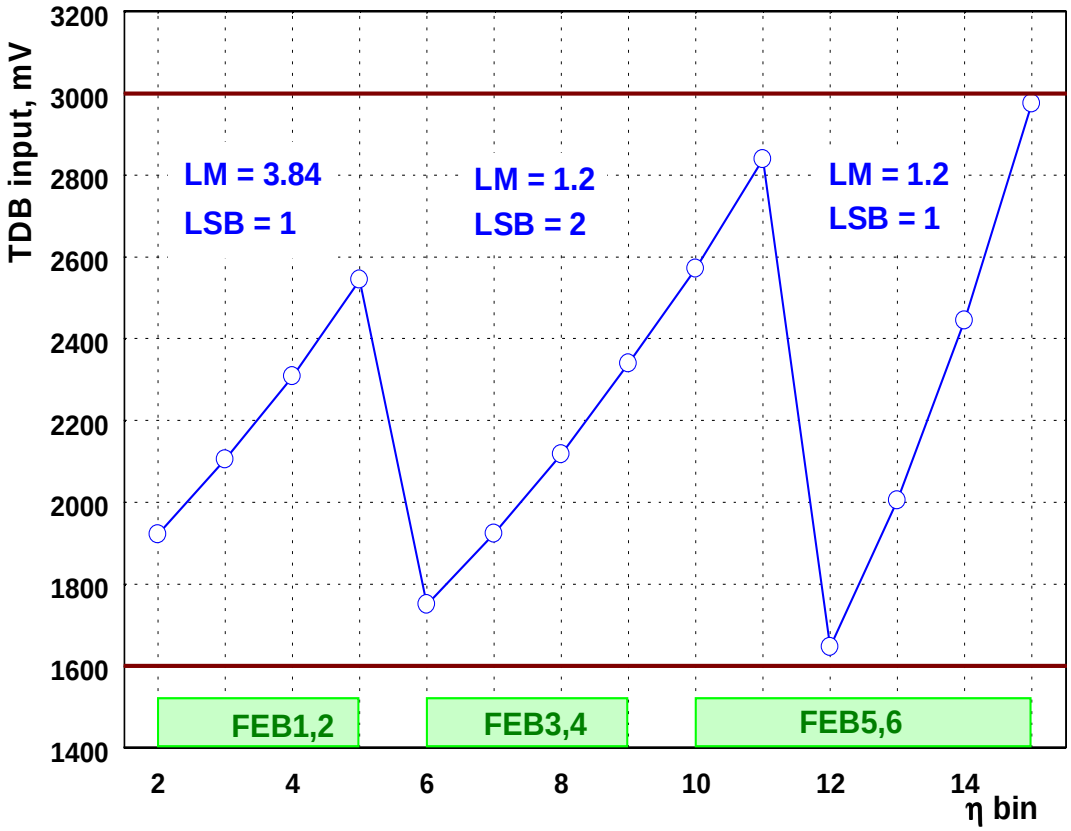


Figure 3: *Amplitude on the TDB input for 14 η-bins calculated for E_T = 256 GeV*

The amplitudes were calculated by using the known ratio between total and visible energy for hadronic shower (26 and 52 for segments 1,2 and 3,4 respectively). The ratio between visible energy and the ionization current is expected to be 7.38 μA/GeV for the ATLAS conditions. This ratio is derived from the HEC test beam data extrapolated to the LAr temperature in the final cryostat. The cold electronics and preshapers are described by the model functions [4]. The LM is considered as an ideal RC-CR shaper with 15 ns shaping time. No signal distortions are produced by LSB and by baseplane.

It can be seen that all amplitudes at the TDB input are already within the window of 1600 – 3000 mV, so that no additional gain adjustment is needed at the TDB level. The absolute value of the amplification (ratio between input amplitude and differential output swing) can be made equal to ~1.

It is known that the trigger cables (from TDB output to L1 cavern) produce significant attenuation of the signal with a factor of 0.6-0.7 [5]. In the case of necessity, this attenuation can be compensated in TDB by increasing its amplification factors. But this solution is not desirable because it leads to increasing the linearity range.

In the HEC channels all signals have the equalized peaking time. This is done by the rise time compensation in the preshaper circuits [6]. The delay of signal propagation in different longitudinal segments is also equalized by a proper choice of the cold cables length [7]. So, any adjustments of the signal timing and delay are not required in the TDB.

1.4 TDB specification requirements

The set of specification requirements to the TDB follows from the electrical characteristics of the input and output loads. The mechanical requirements are determined by the design of the front-end crate [8]. The radiation tolerance and reliability issues are common to all boards in the front-end crate. The list of requirements is given below.

1. TDB has the same dimensions as other front-end boards:
   WxLxH=490x409.5x20.3 mm
2. Power supply from the front-end crate power bars 4 (+7V) and 9 (-7V) similar to the tower builder board
3. Power dissipation is not more then 10-15 W. It allows do not use the cooling plates
4. Input impedance is 50 Ω ±5%
5. High frequency band. Integrating pole not more than 2 ns
6. Gain as output differential to input unipolar amplitudes ratio close to 1 for ~100 Ω output load
7. Gain variation from channel to channel (RMS) not more than 1%
8. Integral nonlinearity better than 1% for the range of amplitudes up to 3V
9. Noise level is low enough to do not increase the total noise by more than 5%
10. Crosstalk is not more than 1%
11. Output impedance in each line 50 Ω
12. Radiation stability up to γ-dose of 350 Gy and neutron fluence of $3.2 \cdot 10^{12}$ n/cm^2

Since the power consumption is expected to be very low, presumably cooling plates are not required. To provide the electromagnetic shielding of the TDB module, the simple aluminium sheets can be used. The TDB is completely analog board, no FPGAs are foreseen, and therefore, the SPAC bus will not be used. TTC signals are also not needed for the TDB operation.

2. TDB design and simulations

2.1 Board layout

The board layout is schematically shown on Fig.4. TDB contains 96 channels placed on one side of PCB. All channels are located near the input connectors J1-J3 in order to minimize the length of the signal transmission from FEB. 6 output connectors J4-J9 are fixed on the front panel, which is screwed on the PCB via 8 aluminium supports. Voltage regulators (if needed) and filters will be placed near the power connector J10.

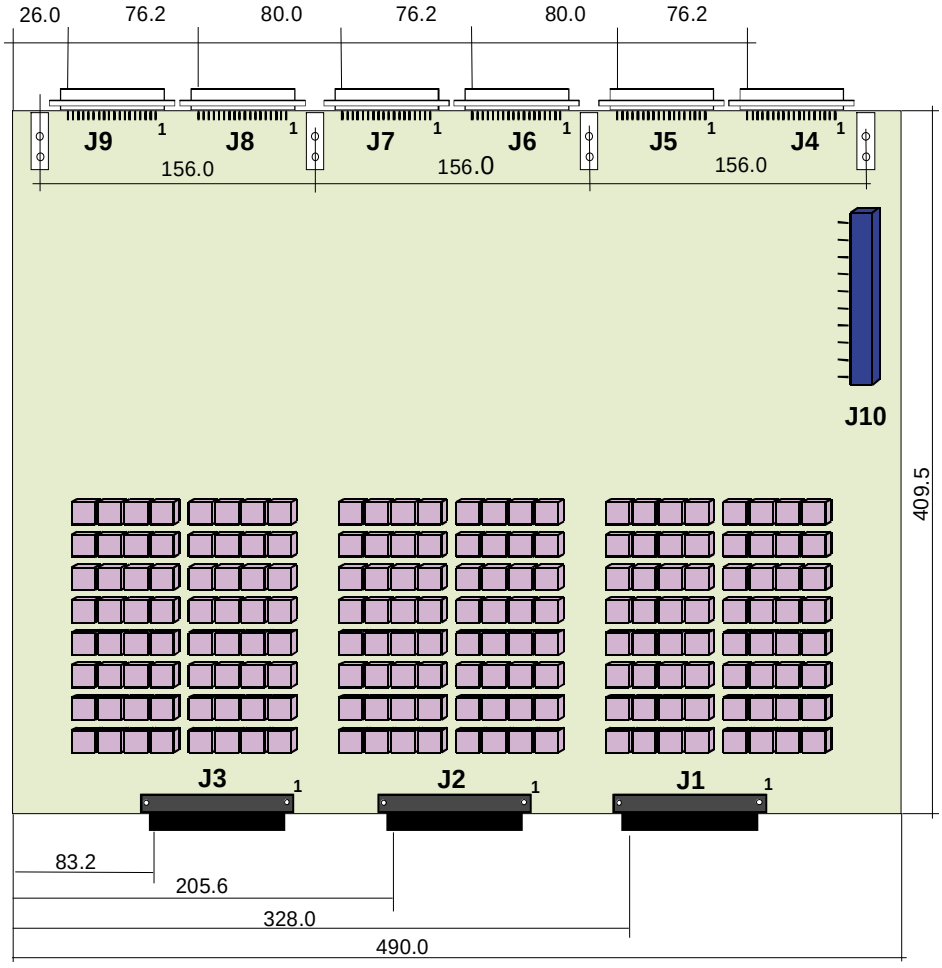


Figure 4: *Layout of the TDB. View from the element side.*

TDB channels are numbered from 0 to 95, the correspondence between channel number and pins of input and output connectors are presented in Tab.2

Table 2: *TDB channels and corresponding pins of input and output connectors.*

TDB ch	J1 pin	J4 ch
0	31	0
1	29	1
2	27	2
3	25	3
4	23	4
5	21	5
6	19	6
7	17	7
8	66	8
9	68	9
10	70	10
11	72	11
12	74	12
13	76	13
14	78	14
15	80	15
	J1 pin	**J5 ch**
16	15	0
17	13	1
18	11	2
19	9	3
20	7	4
21	5	5
22	3	6
23	1	7
24	96	8
25	94	9
26	92	10
27	90	11
28	88	12
29	86	13
30	84	14
31	82	15

TDB ch	J2 pin	J6 ch
32	1	0
33	3	1
34	5	2
35	7	3
36	17	4
37	19	5
38	21	6
39	23	7
40	66	8
41	68	9
42	70	10
43	72	11
44	82	12
45	84	13
46	86	14
47	88	15
	J2 pin	**J7 ch**
48	9	0
49	11	1
50	13	2
51	15	3
52	25	4
53	27	5
54	29	6
55	31	7
56	74	8
57	76	9
58	78	10
59	80	11
60	90	12
61	92	13
62	94	14
63	96	15

TDB ch	J3 pin	J8 ch
64	1	0
65	3	1
66	5	2
67	7	3
68	17	4
69	19	5
70	21	6
71	23	7
72	66	8
73	68	9
74	70	10
75	72	11
76	82	12
77	84	13
78	86	14
79	88	15
	J3 pin	**J9 ch**
80	9	0
81	11	1
82	13	2
83	15	3
84	25	4
85	27	5
86	29	6
87	31	7
88	74	8
89	76	9
90	78	10
91	80	11
92	90	12
93	92	13
94	94	14
95	96	15

Free space of PCB is covered by ground layer on both sides. There are three independent ground areas – TDB ground and two output grounds. The trigger cable has two ground shields – the common shield and individual shields of twisted pairs [8]. Both grounds are connected to special pins of the cable connector as shown on Fig.5. Corresponding to that, there are two additional ground layers on TDB in the region of front panel. The connections of these three ground layers of TDB have been discussed in March 2001 with W.E.Cleland, J.Pascual and V.Radeka. One of the possibility is shown on Fig.6.

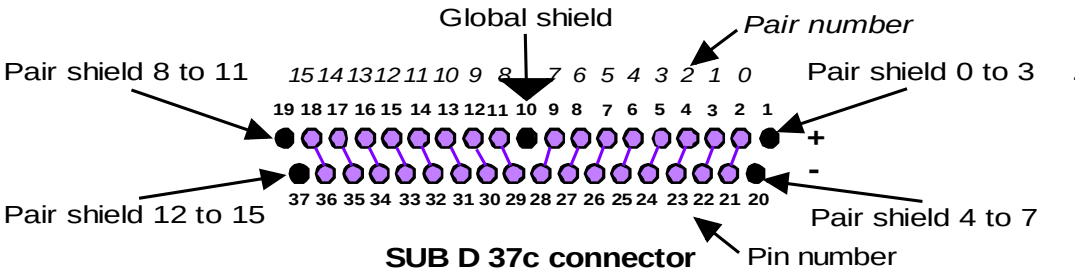


Figure 5: *TDB output connector. Special pins are assigned for global and local shields.*

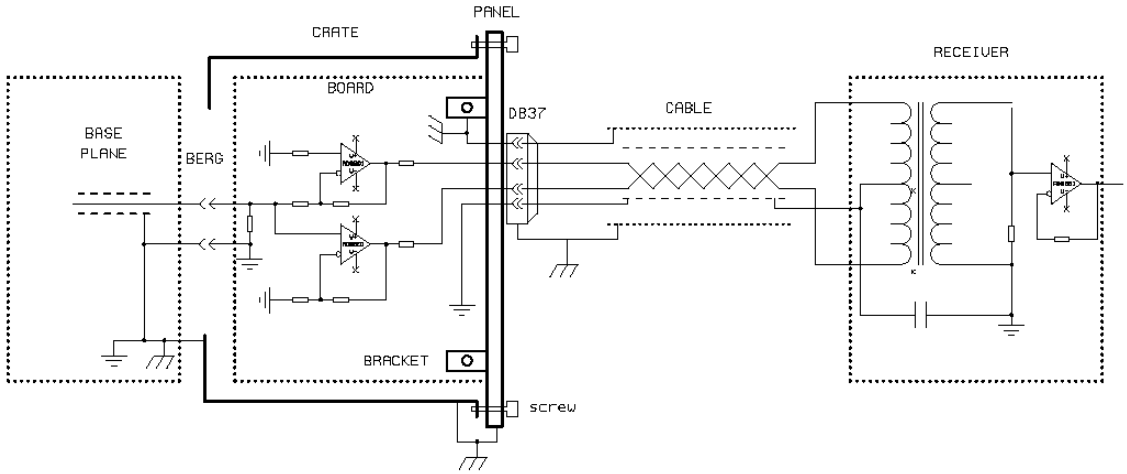


Figure 6: *Connections of ground layers of TDB*

The front panel is connected to the FEC mass through screws and completes the Faraday cage. The trigger cable global shield is connected to the front panel through the connector mass and on the TDB. So the cable shield is a prolongation of the Faraday cage to the trigger cavern. The individual shields of twisted pairs are connected to the TDB analog ground. This connection can be done by jumpers.

The PCB has 6 layers with cross section and dimensions shown on Fig.7.

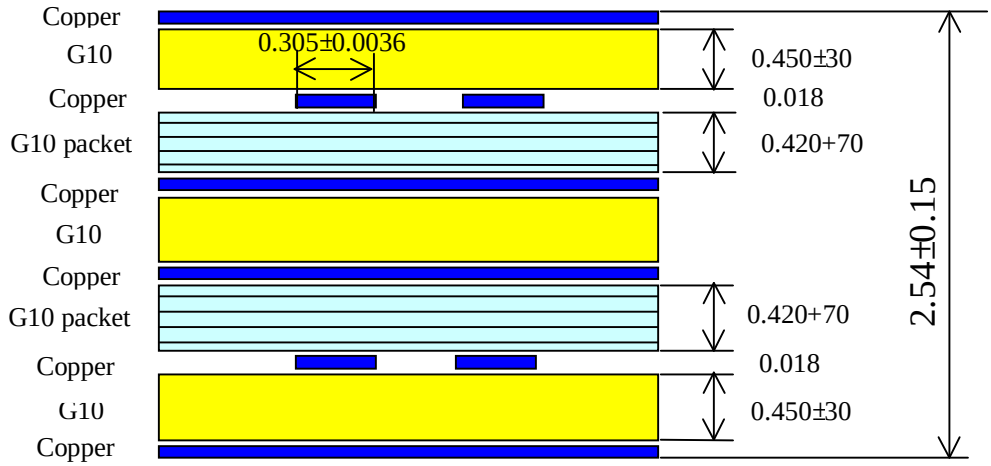


Figure 7: *Cross section of PCB and layers thickness.*

2.2 Channel scheme

The main function of TDB is to transform the unipolar signal coming from LSB to the differential signal and drive the 70 m twisted pair cable. All signal lines on the baseplane and on the FEB have 50 Ω wave impedance. The LSB is designed with the 50Ω output serial resistor in order to achieve approximately the 50 Ω output impedance. That allows a high input impedance of the signal receiver since the reflections are damped by the LSB output. Nevertheless the double termination is more effective, therefore a 50 Ω input receiver is preferable to reduce the effects of reflections.

We made SPICE simulations of two types of TDB channels – with 56 Ω input resistor and without it. Two schematic diagrams are presented on Fig.8. The values of the feedback elements Rf1, Rf2 and Rf3, Rf4 are chosen in such a way to have the same gain factor in both cases. The preshaper, LM, LSB and receiver of trigger signals are represented by Laplace objects with corresponding transfer functions.

The TDB channel is made by using a high frequency low power amplifier circuit AD8001 [9]. This circuit is chosen because it is used in the tower builder board and all pre-selection tests have been already made. All resistors are standard with 1% tolerance. No decoupling capacitors are foreseen both in the input and output stages. The output serial resistors of 50 Ω are introduced to protect amplifiers against shorts. They also increase the stability against possible oscillations in particular if the output load has capacitive component.

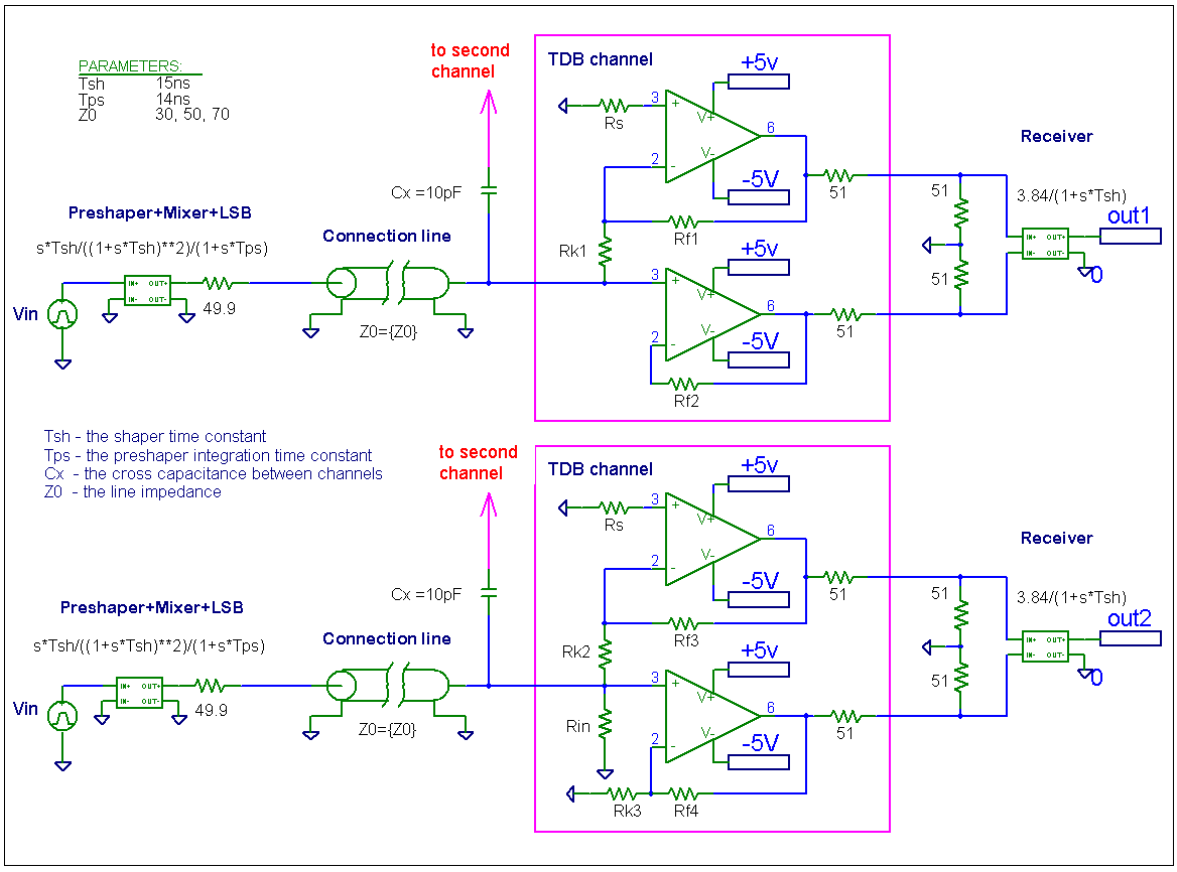


Figure 8: *Schematic diagram used for simulation. The upper part is the channel with high input impedance and the lower part is the channel with 50Ω input resistor.*

2.3 Transfer function and triangular response

The step response of the TDB channel with 50 Ω input resistor is shown on Fig.9. The ideal rectangular pulse is applied directly on the channel input. The output pulse is the difference of positive and negative signals. The rise time from 0.1 to 0.9 of amplitude reconstructed from this plot is 1.2 ns, that corresponds to an integration pole of approximately 0.5 ns. This value is sufficiently small and therefore TDB does not contribute to the final shape of the trigger signal. The transfer coefficient is 0.987. A small overshoot of ~1% can be seen in the signal beginning.

The response of the full trigger chain to the triangular ionization pulse has been simulated for two types of the TDB chain. In both cases the path from LSB to the TDB input is considered as ideal transmission line with wave impedance Zo having nominal value of 50 Ω. The length of this line is 2.5 ns that corresponds to the longest path from FEB to TDB. The HEC chain is described by Laplace objects with transfer functions taken from [4] with nominal parameters of cold electronics and preshaper. The gain of LM and LSB are chosen as 1.2 and 1.0. No signal attenuation and distortion in the long trigger cable is modelled.

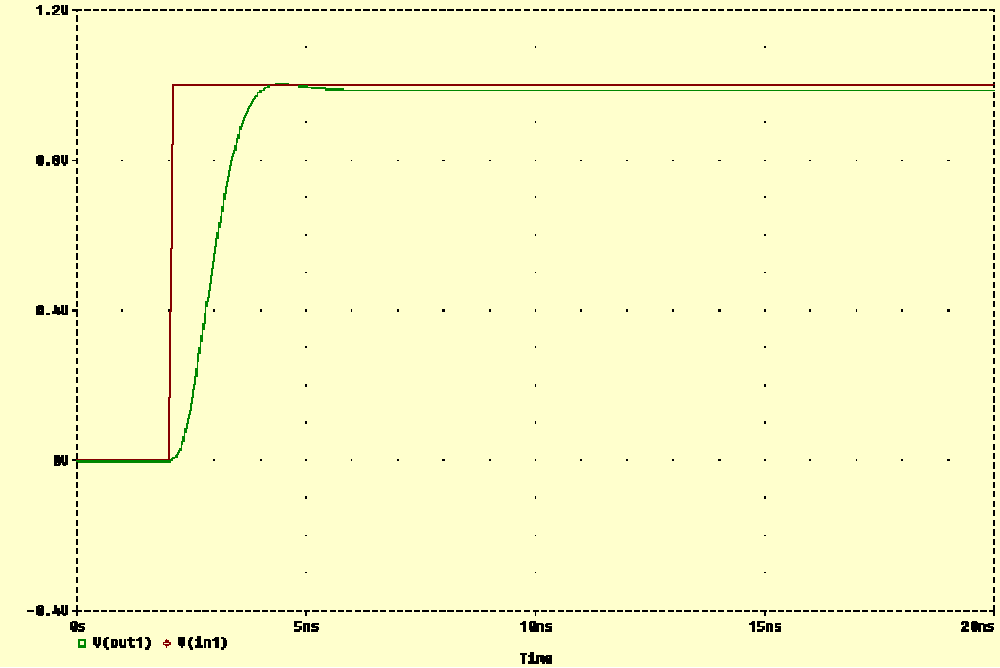


Figure 9: *Step response of the TDB channel. Output signal is the difference of positive and negative outputs.*

Fig.10 shows signals for the case of the TDB chain with high input impedance. The amplitude at the receiver output is 388 mV for the ionization current of 100 μA, that gives conversion factor of 1.1 mV per total energy 1GeV deposited in the trigger tower. In order to estimate the effect of baseplane mismatching, the simulations were done for 3 values of the line impedance – 30, 50 and 70 Ω. It can be seen that reflections give not very big contribution to the waveform parameters. The line impedance variation of ±5Ω produces the amplitude degradation of ±0.2% and peaking time variation of ±0.35 ns.

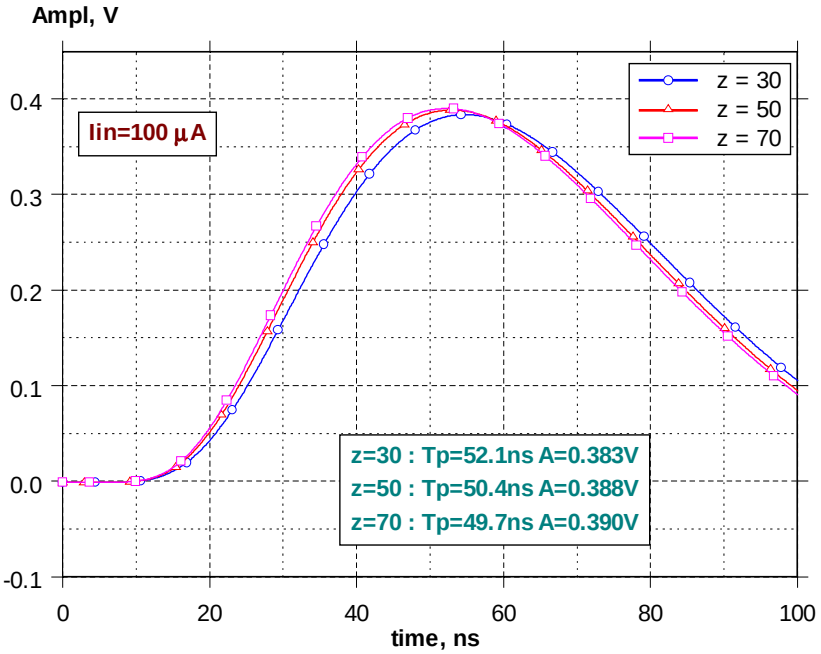


Figure 10: *Triangle response of the channel with high input impedance. Signals are given at the receiver output. Simulations done for the line impedance Zo = 30, 50 and 70 Ω Tp and A being the signal peaking time and amplitude.*

The case of the TDB channel with low input impedance is shown on Fig.11. For the nominal line impedance, amplitudes have the same values as in the previous case and peaking time is a bit shorter. The effect of the reflections is practically not seen due to the damping on both ends of the line.

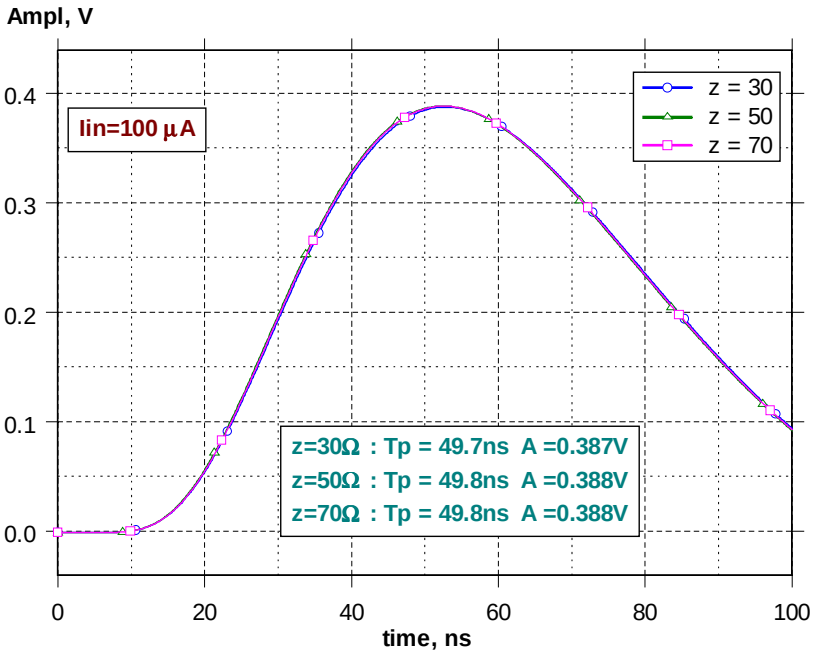


Figure 11*: Triangle response of the channel with 50 Ω input impedance. Signals are given at the receiver output. Simulations done for the line impedance Zo = 30, 50 and 70 Ω Tp and A being the signal peaking time and amplitude.*

It can be expected that the line termination conditions affect also the inter-channel crosstalk value when the crosstalk appears due to a coupling to the input of TDB channel. This coupling can be produced by a parasitic capacitance between neighbouring lines on the baseplane or on the PCB. In the case of the high input impedance circuit, the total input load is twice higher that results in the twice bigger crosstalk amplitude.

Fig.12 shows the crosstalk signal due to the inter-channel capacitance of 10 pF. This value is not based on knowledge of real environment, this is just a guess value. The crosstalk signal has a shape, which is the time derivative of original signal. Its amplitude is proportional to the crosstalk capacitance value. Vertical scale on Fig.12 is expressed in % to the main signal amplitude. The crosstalk amplitude is 1% in the case of double line termination and twice higher for the circuit with high input impedance.

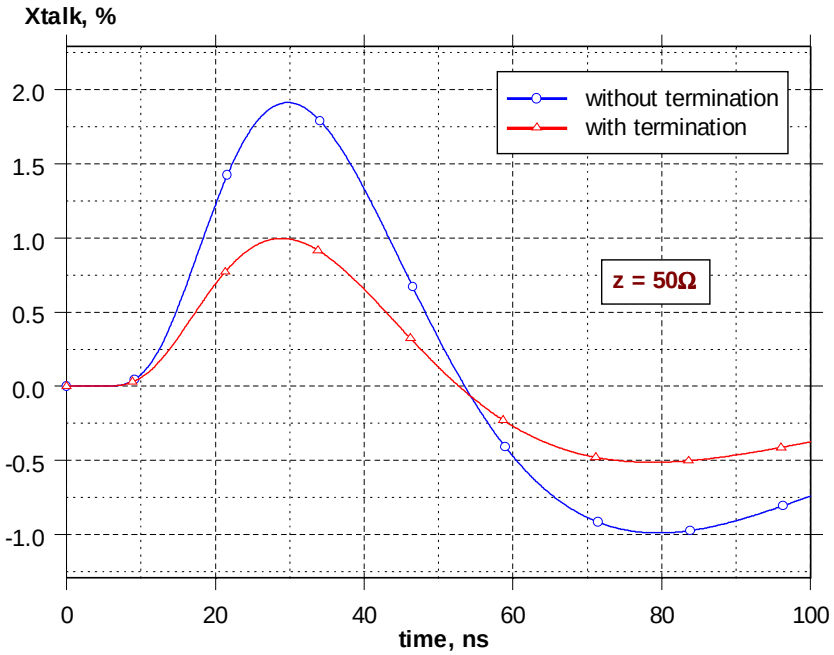


Figure 12: *Crosstalk to the nearest channel for the TDB channel with high input impedance and with 50 Ω line termination.*

2.4 Input and output impedance

The simulated input impedance as a function of frequency is shown on the left plot of Fig.13 for the channel without termination. The typical value is 1 kΩ in the working frequency range around 10 MHz. When 56 Ω resistor is introduced in the channel input, the resulting impedance is 50.5 Ω up to frequency of ~300 MHz.

The output impedance for differential signal is presented on Fig.14. It does not depend on the input load and typically equal to 102 Ω in the working frequency range. A difference can be seen in the high frequency region.

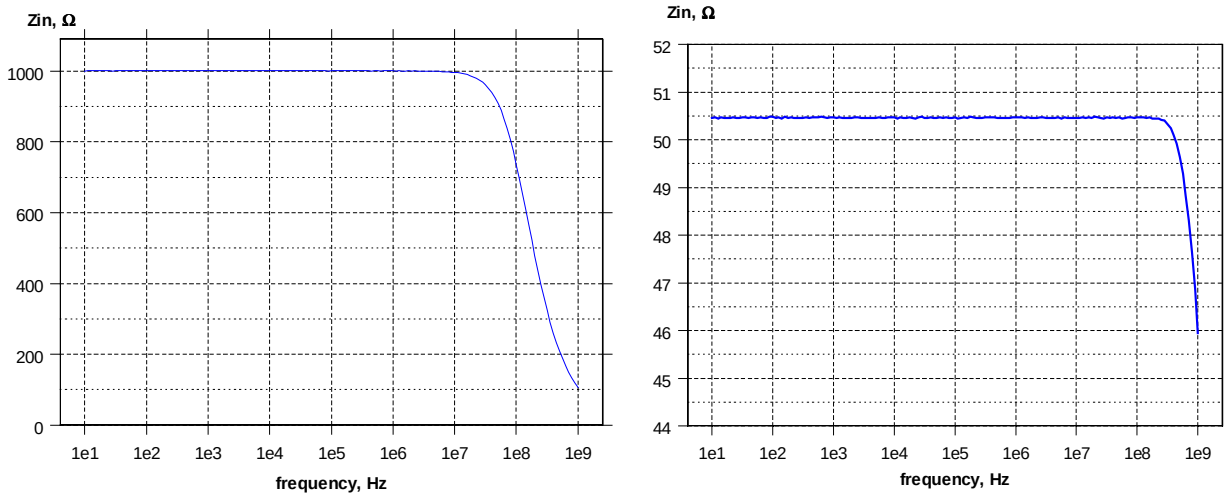


***Figure 13**: Input impedance for open input (left plot and for the case of termination (right plot).*

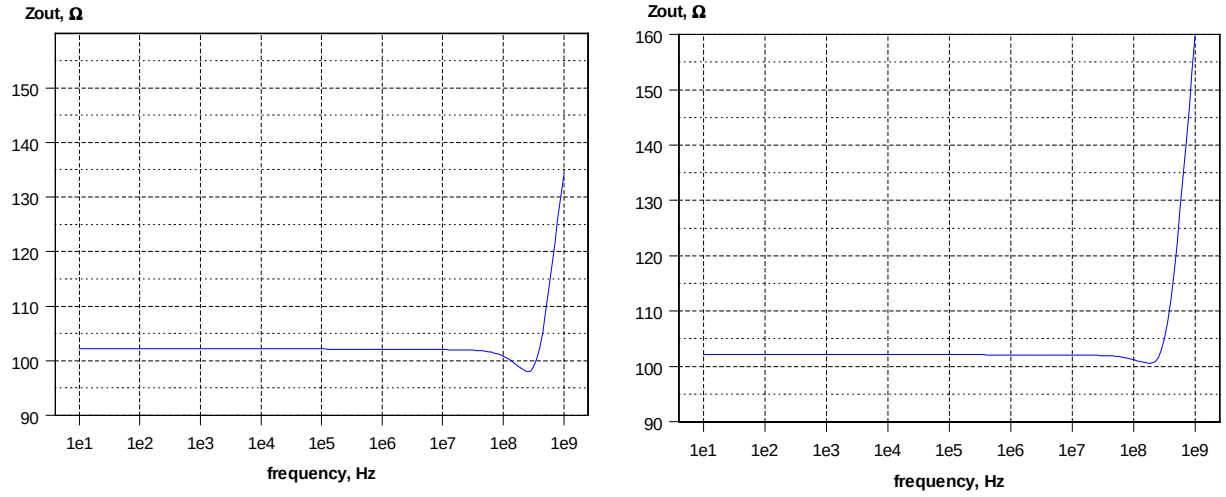


***Figure 14:** Output impedance for open input (left plot) and for the case of termination (right plot).*

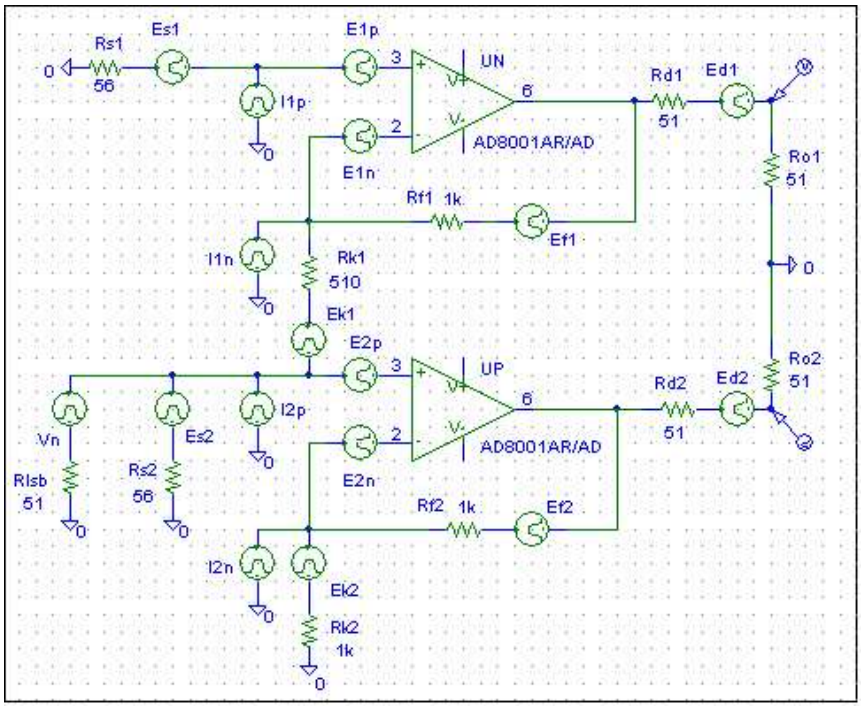
2.5 Intrinsic noise

The intrinsic noise of the TDB channel is estimated by using the data sheet values for the noise voltage and noise current of AD8001 circuit. They are 2 nV/√Hz for the serial noise, 20 pA/√Hz for the negative current and 4 pA/√Hz for the positive one [9]. These values are considered as frequency independent. The thermal noise of resistors is described by well-known Nyquist expression. All sources taken into account in the following calculations are shown on Fig.15. The transfer coefficients from each source to two output points are obtained by SPICE simulations and presented in table of Fig.15.

The total differential response is the sum of two columns of the table. Response to input signal is 0.98, so the equivalent input noise is practically equal to the output noise. The output noise spectral density is the quadratic sum of all 16 components enlisted in the table:

$$\frac{d}{df}V_d^2 = \sum_{k=1}^{16} G_k^2 \cdot \frac{d}{df}V_k^2$$

Where G_k are transfer coefficients and V_k are noise of corresponding sources. In the case of current, the transfer coefficients are measured in kΩ.



source	Out1	Out2
Vin	-0.485	0.494
E1p	-1.420	-0.049
E1n	1.426	0.047
I1p	-0.079	0
I1n	0.498	0
Es1	-1.420	-0.049
Ek1	-0.927	-0.049
Ef1	-0.498	0
Ed1	-0.499	0
E2p	0	-0.992
E2n	0	0.996
I2p	0.025	-0.025
I2n	0	0.498
Es2	-0.442	0.450
Ek2	0	-0.498
Ef2	0	-0.498
Ed2	0	-0.500

Figure 15: *Noise sources of the TDB channel (diagram) and their transfer coefficients to the output points (table).*

The output noise spectral density for room temperature is equal to 15.6 nV/√Hz and mainly comes from the negative current of operational amplifiers. The RMS noise voltage depends on the frequency band of the upcoming filter. In the receiver station there is one integrator with 15 ns shaping time. The noise RMS value for this condition can be calculated as follows:

$$\left\langle V_d^2 \right\rangle = \int_0^\infty \frac{S(\omega)}{1+(\omega\tau)^2}\frac{d\omega}{2\pi}$$

Since output spectral density is frequency independent, the integral can be easily calculated. The result is:

$$\left\langle V_d^2 \right\rangle = S / 4\tau$$

That gives the RMS value of 64 μV. For the case of TDB channel with high input impedance, the RMS output noise voltage is very close to the previous value.

The main noise source in the HEC electronics chain is the thermal noise of GaAs preamplifiers. Its value varies from tower to tower because of the detector capacitance variations and due to different number of preamplifiers involved. The expected value for the lowest gain in LM and in LSB is 0.5 – 2 mV for summing of 3 longitudinal segments. So, in the worst case the TDB increases the total noise by some 1-2 %.

2.6 Stability to oscillations

Stability of the TDB chain is provided by following the supplier recommendations for the schematics and values of external components. For instance, the output serial resistors effectively damp oscillations in the case of capacitive load. In the TDB chain the 51 Ω resistors are used.

The channel stability was checked by using Bode diagram obtained by SPICE simulations. A linear circuit is stable if the phase between output and input signals is less than 180º at unit-gain frequency. The TDB channel consists of two parts, inverting and noninverting amplifiers. The simulation has been done for both parts separately. Bode plots for the noninverting amplifier is shown on Fig.16, very similar result is obtained for the inverting part. It can be seen that the unit gain is reached at frequency of 3 GHz and the phase rotation at this frequency is 170 degrees, that grants some safety margin in stability.

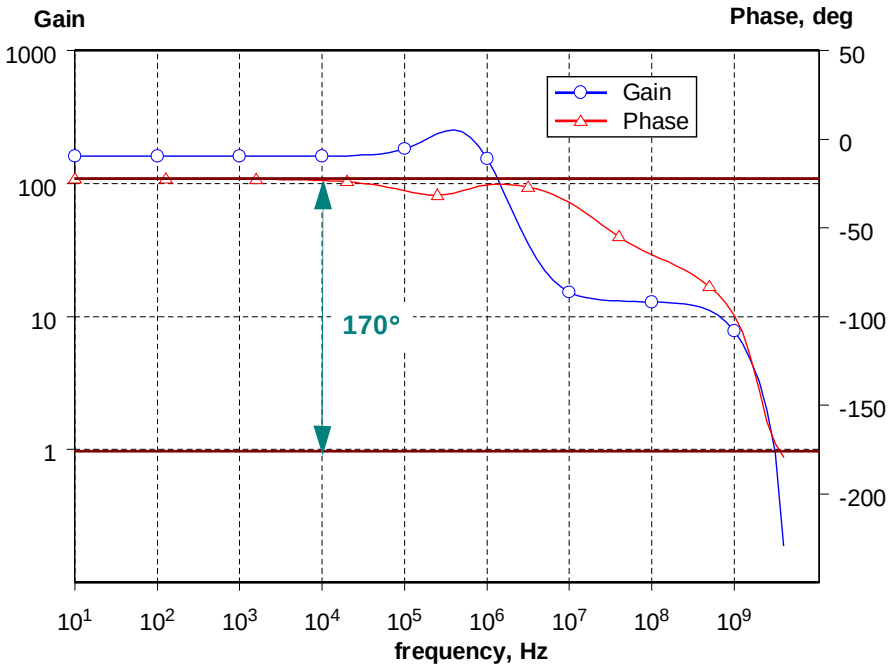


Figure 16: *Bode plot for the inverting output of the TDB channel.*

It is known that the results of the stability simulations depend strongly on the circuit model. The curves on Fig.16 are produced for the Analog Device AD8001AR/AD model. Other models available at MPI show similar results.

2.7 Power consumption

The consuming power is very important for the TDB since the usage of standard cooling plates is problematic. Practically all the front panel space is occupied by the output connectors so, there is not enough room for the water plug. A small heating produced by TDB will be taken out by the cooling plates of the neighbouring front-end boards.

The TDB power consumption can be easily estimated by using specification data of the amplifier circuit. The consuming current is 5.5 mA for bias voltages of ±6 V and therefore all 192 amplifiers of the TDB require 1.056A from both power lines. The total dissipating power is 12.67W distributed over the big area of at least ~500 cm^2. No warming is expected under these conditions, so a special cooling is not needed.

3. Tests of prototype boards

3.1 Small prototype board and functional tests

The first prototype of the TDB has been designed in year 2000. This board is a 1/3 part of the full board. It has 1 of 3 input connectors, 32 channels and 2 output connectors with mapping corresponding to connectors J3 and J8, J9 (see layout on Fig.4). The resistors (see bottom diagram on Fig.8) has been chosen as follows: Rin = 56 Ω, Rs = 0, Rk = 510 Ω, Rf = 1 kΩ. A photograph of this board can be seen on Fig.17. Two such boards have been produced and tested in laboratory conditions and in the HEC test beam setup.

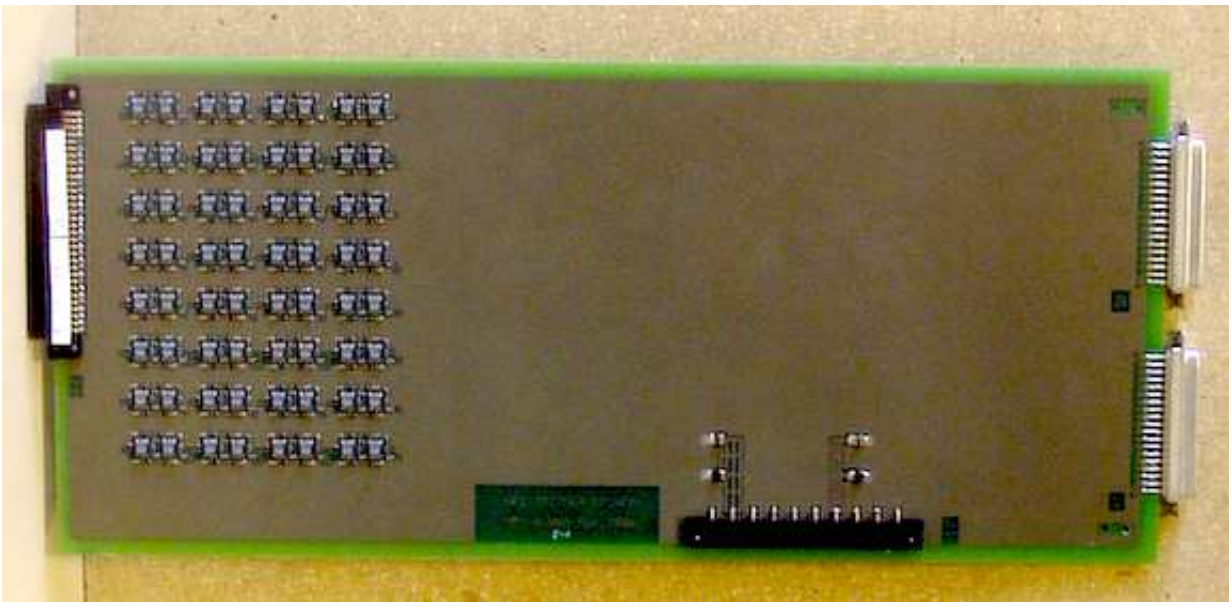


Figure 17: *The first prototype of the TDB. It has 1/3 size of the final board.*

The functional tests have been performed by using rectangular pulse generator and digital oscilloscope. The TDB input signal is formed by using a passive R-C network in order to produce shape close to the shape of the real signals. Fig.18 shows typical input signal and the TDB

differential output. The LSB serial resistors were not emulated in the measuring setup that is why the output signal is twice higher than the input one.

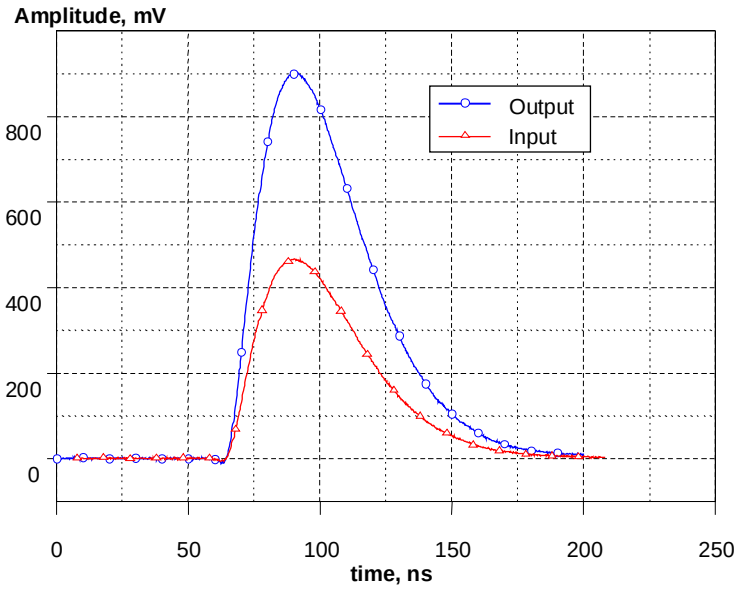


Figure 18: *Measured input TDB signal and differential output in the functional test setup.*

The TDB channel is parameterized by a DC gain G_{TD} and one pole with time constant τ_{TD}. These parameters were reconstructed from comparison of the input and output waveforms. The result is shown on Fig.19. The gain G_{TD} was divided by factor 2 in order to represent the effect of LSB serial resistors. It was found that the gain factor is 0.973 that is very close to the expected value. The integration time constant is 1.2 ns that is twice higher than SPICE value. This can be explained by additional integration in the measuring setup or systematic shifts in the fitting procedure.

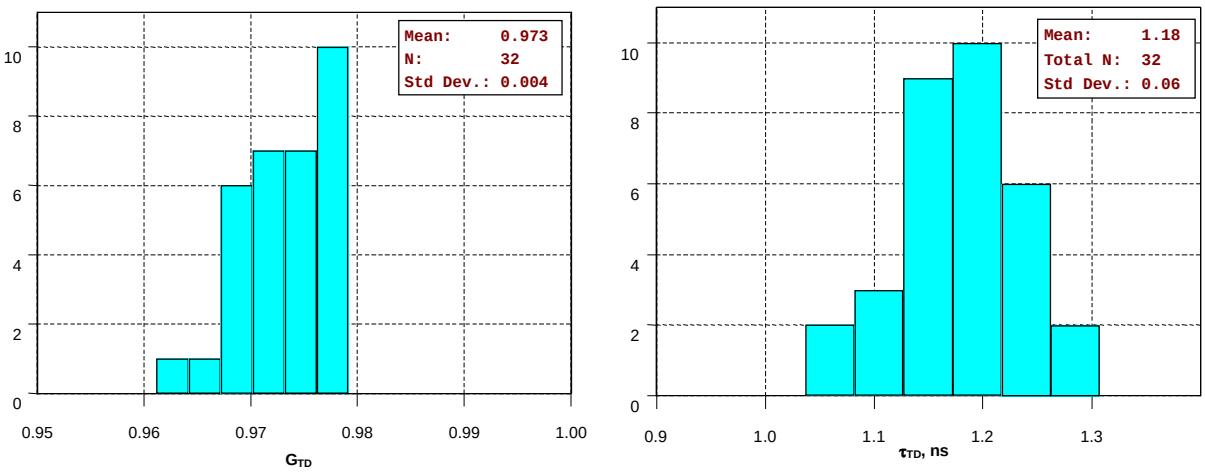


Figure 19: *Distribution of gain and integration time constant for 32 TDB channels.*

The crosstalk in the neighbouring channel is ~0.3% and its shape looks like time derivative of the main signal with the same polarity. Comparing to SPICE results (Fig.12) one can conclude that the inter-channel capacitance is effectively equal to ~3 pF. No crosstalk has been observed in not neighbouring channels.

Measured linearity for one of the TDB channels is presented on Fig.20. It has been found that the linearity range for input signal is 2.8V for 5V bias and exceeds 3.0V for 5.5V bias. In the last case the nonlinearity is 0.3% in the range of 0 – 3.0V.

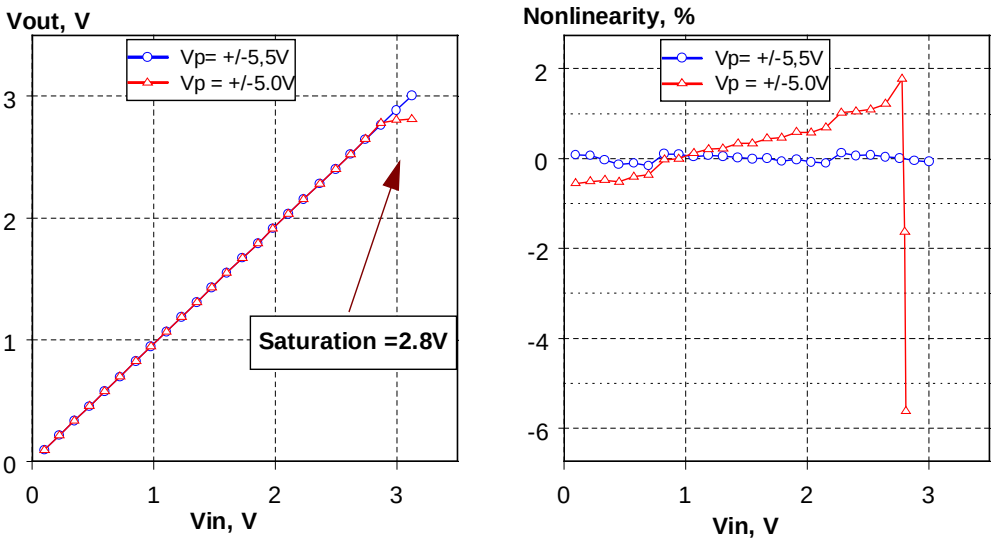


Figure 20: *Linearity ramp (left plot) and nonlinearity value (right plot) for two bias voltages.*

It has been observed that the noise RMS at the negative output is about 2 mV while the positive output has much less value. This indicates a presence of some oscillations in the inverting part of the circuit. It was found that a serial resistor Rs (see Fig.8) of some 10 Ω at the amplifier positive input damps efficiently these oscillations. When 56 Ω resistor was introduced, the noise RMS value at the circuit negative output came down to approximately the same value as at the positive output.

The noise RMS value has been measured by digital oscilloscope and found to be 150-160 μV on the TDB differential output. The expected value can be obtained from theoretical noise spectral density of 15.6 nV/$\sqrt{Hz}$ (p.13). The oscilloscope frequency band of 500 MHz corresponds to the integration time constant of 0.32 ns, the TDB pole is 1.2 ns. In addition, the measuring setup has integration of the order of 1 ns. The resulting frequency band in the noise measurements can be estimated as 2-2.5 ns. Using this value in the equation on p.14, one can estimate the noise RMS value as 150-170 μV that is in reasonable agreement with measurements.

3.2 HEC beam setup and TDB tests in 2000

Two prototype boards have been studied in the HEC test beam facility in July-August 2000 beam period. 6 HEC modules (3 ϕ-wedges) were equipped by final ATLAS cold electronics. The readout was done by 3 FEB vs.-1 where only analog part is present. The preshapers of vs.0 have

been used, they have longer integration time than the final ATLAS version. The shapers were configured to middle gain (~9.2 in our case) for readout output and LM gain was 3.5. All 4 shaper channels are summed to the LM output. The digitization was made by home-made fast ADC modules with 40 MHz clock. One 32-channel ADC module has been allocated to readout TDB output signals.

The beam area occupies low-η region covered by FEB1 and this FEB was equipped by two LSB of S1x16H type with gain 2. 24 trigger towers were available for studies, not all of them are reachable by beam. During the beam period a few dedicated calibration and physics runs have been performed. That time one 70-m trigger cable was available and some measurements have been done with this cable. Fig.21 shows the calibration signal from one of the trigger channels measured with and without long cable.

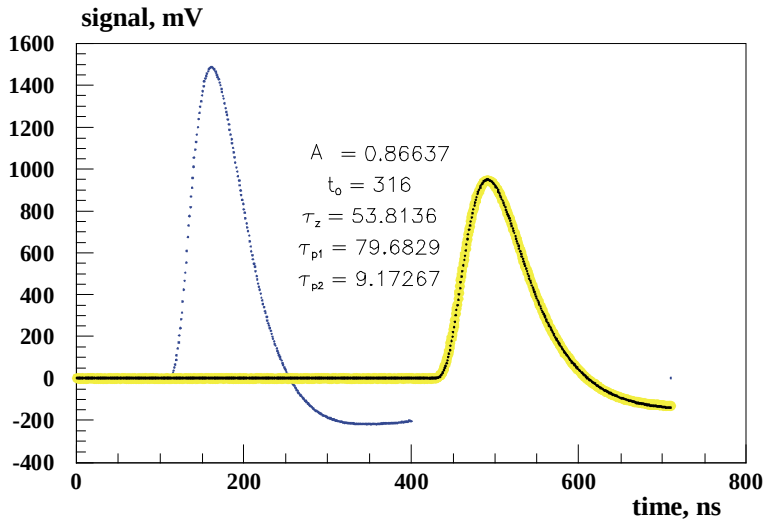


Figure 21: *Calibration signal measured on the TDB output connected to ADC by a short cable (left waveform) and by 70-m trigger cable (right).*

The studies of trigger cable was interesting in view of the further developments of the trigger chain model. The signal distortion in the cable was parameterized in frequency domain by a simple function consisting of attenuation factor a_{TC}, one zero and two poles. So, the cable transfer function in Laplace domain $H_{TC}(s)$ is the following:

$$H_{TC}(s) = \frac{a_{TC} \cdot (1 + s \cdot \tau_Z)}{(1 + s \cdot \tau_{P1}) \cdot (1 + s \cdot \tau_{P2})}$$

The parameters of this function reconstructed from calibration signals in 24 trigger towers are summarized in Tab.3.

Measurements of the noise show that the RMS value is close to the quadratic sum of contributions from 4 readout cells summed to one TDB channel if the difference in shaping functions is taken into account. The analysis of autocorrelation functions indicates no oscillations.

***Table 3**: Parameters of the level 1 trigger cable transfer function.*

parameter	Mean	RMS
a_{TC}	0.868	0.004
τ_{P1}	80.8	6.5
τ_{P2}	9.9	1.8
τ_{Z}	55.7	5.8

The crosstalk between neighbouring trigger towers is mainly due to the resistive coupling in the calorimeter electrodes. It is known that its value is few percents depending on the padboard resistivity and pad dimensions. For the trigger towers without this coupling, the typical crosstalk is –0.7%, mainly coming from cold electronics and FEB components.

3.3 Full size prototype board

After the small board was studied, a full size prototype has been designed. Two boards were produced and fully equipped in year 2001. They were tested in laboratory conditions and in the HEC beam setup during August-2001 beam period. Its picture is shown on Fig.22. The board has 96 channels with the same schematics as in the small prototype board. The only change is that resistor Rs = 56 Ω was introduced (see bottom diagram on Fig.8) in order to increase the circuit stability.

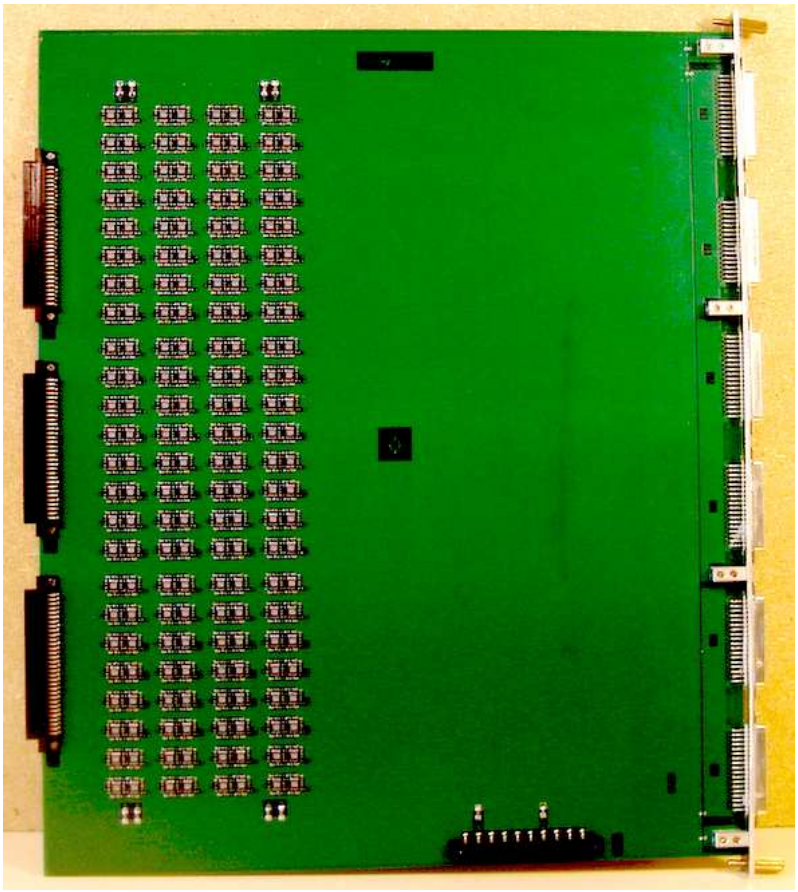


***Figure 22:** Top (element) side view of the full size TDB prototype*

The mapping from input to output connectors has been also changed with respect to the small prototype, because it was recognized meantime that the numbering order of the input connector was inverse. The board is equipped by aluminium front panel presented on Fig.23. Output connectors of DB37 type are fixed by screws. The board has the final ATLAS dimensions, but the side shields are not foreseen.

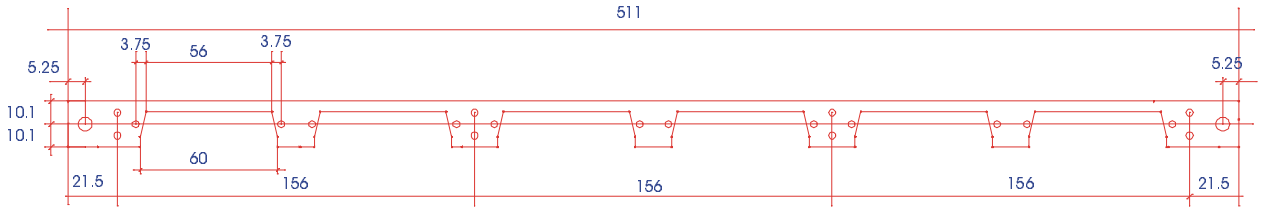


Figure 23: *Drawing of the TDB front panel.*

There are three separated layers for analog TDB ground, global trigger cable shield and for individual twisted pair shields. The first one occupies almost all space on both sides of PCB. The common output ground is a 1.5 cm wide strip on the bottom side along the front panel. This area is connected to J4-J9 ground pins and to the front panel. The third ground is also a 1.5 cm wide strip but on the top side of PCB. It is connected to corresponding pins of J4-J9 connectors. The connection between three grounds can be done if necessary by jumpers or capacitors. Special metallized holes are foreseen for this connection.

3.4 Laboratory functional tests

The functionality has been evaluated in laboratory conditions. The gain and integration pole were determined by measuring step response. Similar to the small prototype measurements, the serial 51 Ω resistors of the LSB output were not represented in the measuring setup, so the TDB output signal is twice higher than in real environment. Fig.24 shows the step response for two channels determined as difference of two output points.

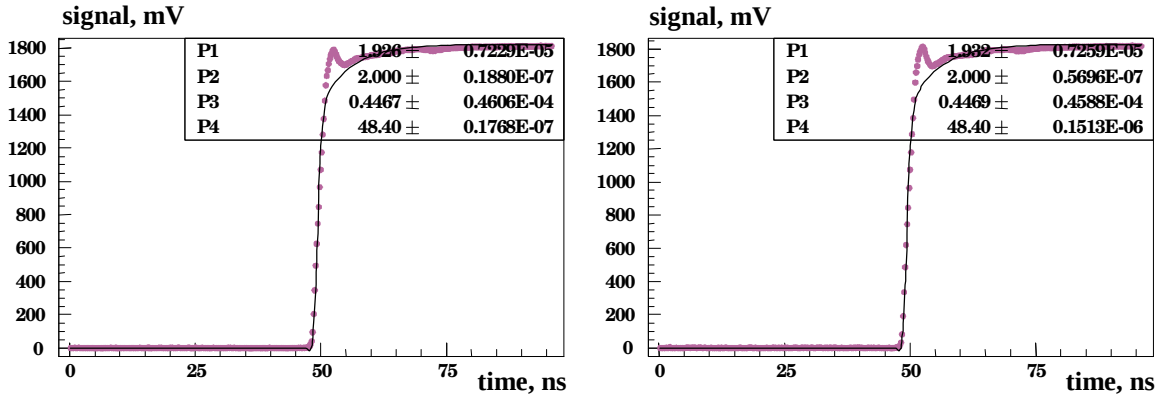


Figure 24: *Typical step response and fit by 1-pole and 1-zero function.*

The input signal from rectangular pulse generator has some overshoot in the pulse rising edge. This overshoot is seen also on the TDB output. It makes difficult to reconstruct the TDB rise time reliably. In order to describe better this complicated shape, one additional zero was introduced to the function which was used to fit data. This time constant was extracted from the input waveform and fixed to 2 ns. Since the same cables have been used in all measurements, the signal origin was also fixed. Two free parameters of the fit are gain (parameter P1) and rise time τ_{TD} (P3). The TDB gain G_{TD} is defined as P1/2. Distributions of these two parameters for 96 channels of one TDB are presented on Fig.25.

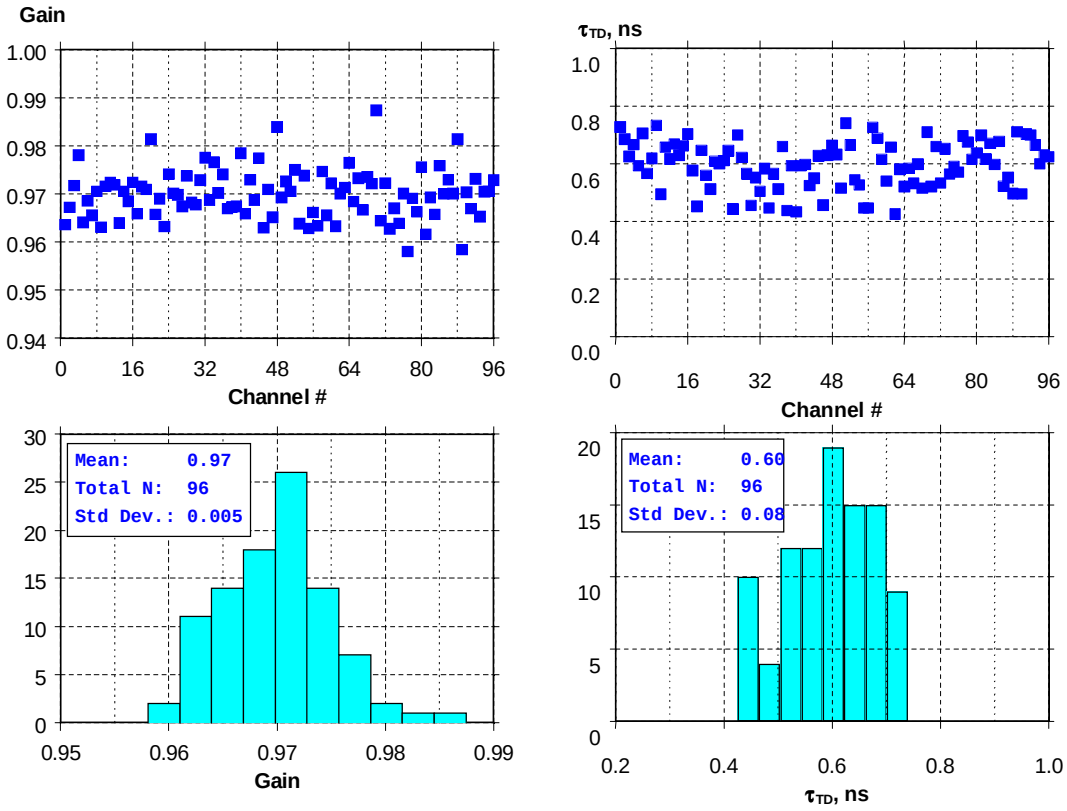


Figure 25: *The TDB gain (left plots) and rise time (right) of one board*

The crosstalk between neighbouring channels is less than 0.5% when measured with rectangular input signal. The RMS of output noise is at the level of 150 μV. The integral nonlinearity is usually less than 0.5% up to 3V of output voltage swing with external power supply voltages of ±6V.

3.5 Test beam results in 2001

The full size TDB prototype has been tested in the same beam environment as the small board. In year 2001 FEBs have been equipped by the new version of preshapers of final ATLAS design. During the August-2001 a few dedicated calibration and physics runs have been performed. The TDB output and FEB output signals have been digitized simultaneously. It gives possibility to compare directly the readout and trigger chain. Only one FEB was equipped by two LSB of S1x16H type, so only 24 trigger towers have been studied. The side view of one of the HEC

modules is shown on Fig.26. The trigger towers connected to TDB (low η region) are numbered from 1 to 24.

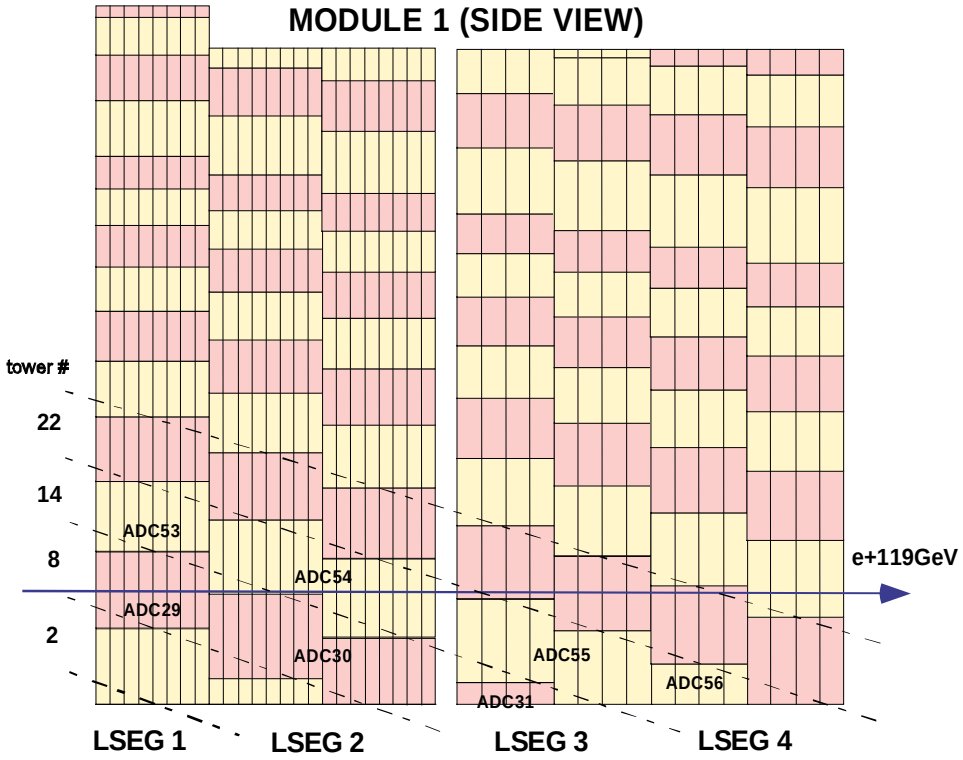


Figure 26: *Side view of one of three HEC wedges. Trigger towers connected to TDB are numbered from 1 to 24.*

The noise has been measured with calibration triggers. Fig.27 presents the RMS value measured directly on the TDB output (blue circles). The noise in ATLAS conditions is smaller because of the additional integration in receiver station. This integration gives typically a factor of 0.77 for the RMS value. The noise in the case of receiver (rose squares) is estimated simply by multiplying the TDB RMS by this factor. This noise can be compared with the noise seen in the readout chain (green triangles). This noise was calculated as quadratic sum of RMS values in corresponding readout channels. The difference in gain factors was also taken into account.

It can be seen that the TDB noise is systematically higher then in the readout chain. This is because in the real setup there is a small correlation between channels, so that the pure quadratic sum of RMS values gives an underestimation of the noise in trigger chain. It is known that FEB-1 has big excess (coherent) noise in the $\eta = 1.55$ region. This is due to the interference from digitizing system. This effect can be clearly seen in the left part of the plot where the TDB noise is significantly higher than the noise of readout chain.

The excess noise is also seen in the autocorrelation functions presented on Fig.28. These functions were calculated from waveforms measured by digital oscilloscope with 1 ns digitization period. The oscillating term is bigger at the FEB edge (tower 2) and becomes smaller for channels that are far from the edge. It is practically disappears in the tower 6.

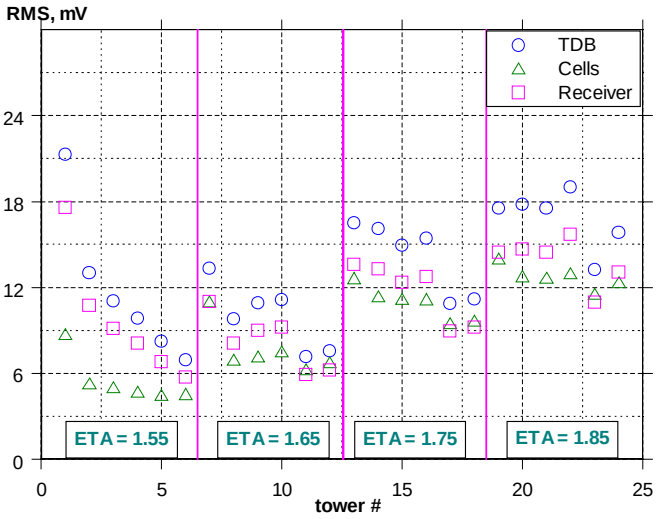


Figure 27: *Noise RMS value measured on the TDB output (circles), recalculated to the case of receiver (squares) and corresponding noise in the readout chain (triangles).*

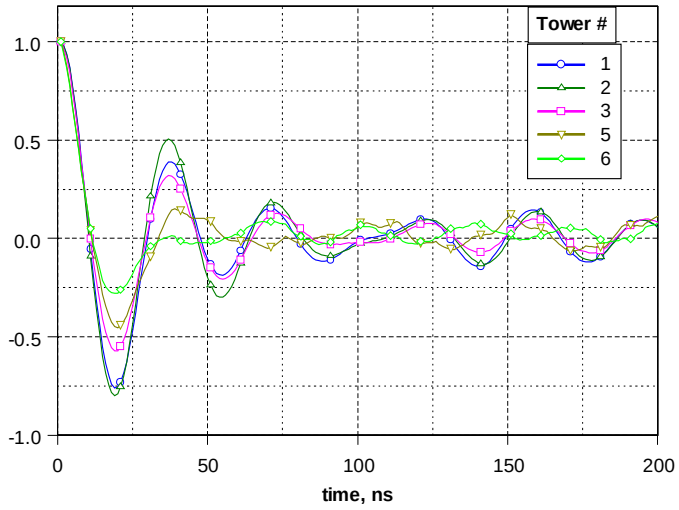


Figure 28: *Noise autocorrelation functions obtained from oscilloscope measurements.*

The trigger signals have been measured mainly with standard HEC calibration when cells are pulsed sequentially turning the calibration generators one by one. In this mode of calibration, the response of TDB to individual cells can be studied. Fig.29 shows the response of 24 trigger channels. For each channel the response is calculated as average of amplitudes over cells going to the corresponding trigger sum. The mean value of this histogram is normalized to 1. The full spread is $\pm$ 4% and sigma of this distribution is 2.4%. It gives an evaluation of the uniformity of amplitudes in the HEC trigger system.

In order to estimate the peaking time of trigger signals in the level-1 preprocessor, the measured waveforms were convoluted with theoretical receiver transfer function (integration with

14 ns time constant). The peaking time of these predicted signals is shown on Fig.30 separately for each readout cell and for trigger signal (open circles), which is calculated as the sum of corresponding readout signals. 24 trigger waveforms have average peaking time of 53 ns with variance of 1.2 ns.

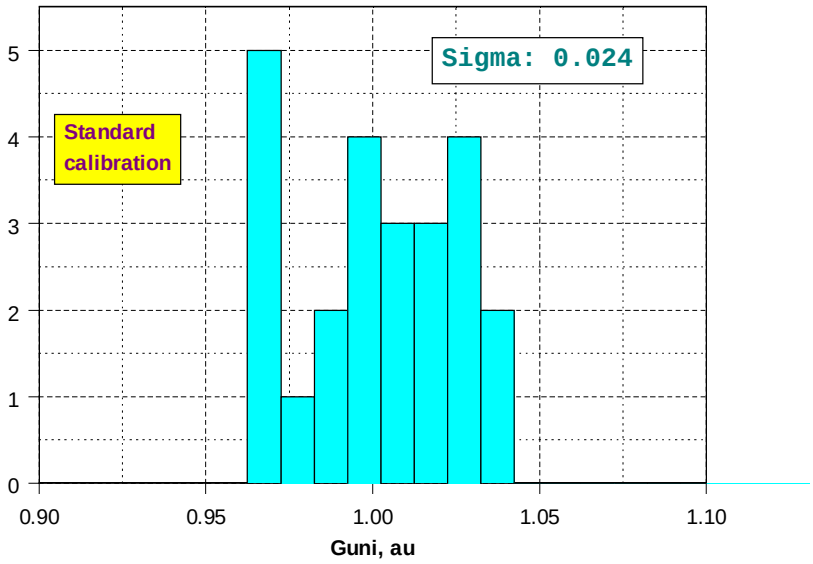


Figure 29: *Distribution of amplitudes in 24 trigger channels. The histogram is normalized to mean value = 1.*

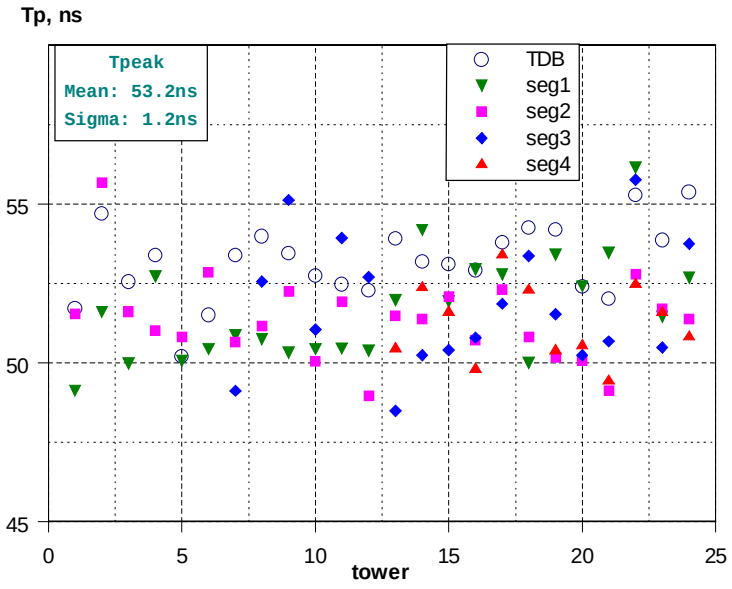


Figure 30: *Peaking time of trigger signals (circles) and signals from corresponding readout cells.*

During the test beam period a few physics runs with electrons of 119 GeV have been taken. The main energy was deposited in the first cell of tower number 8 with some leakage to the cell ADC54 of the neighbouring tower 14. Signals in these two towers and in corresponding readout cells are shown on Fig.31. The maximal signal is in the readout cell ADC29 and in trigger tower 8 (right plot). The energy leakage to the cell ADC54 and corresponding tower 14 produces small signals (left plot). Crosstalk signal due to resistive coupling on the HEC padboard can be seen in ADC53. There are no signals in the rear HEC module.

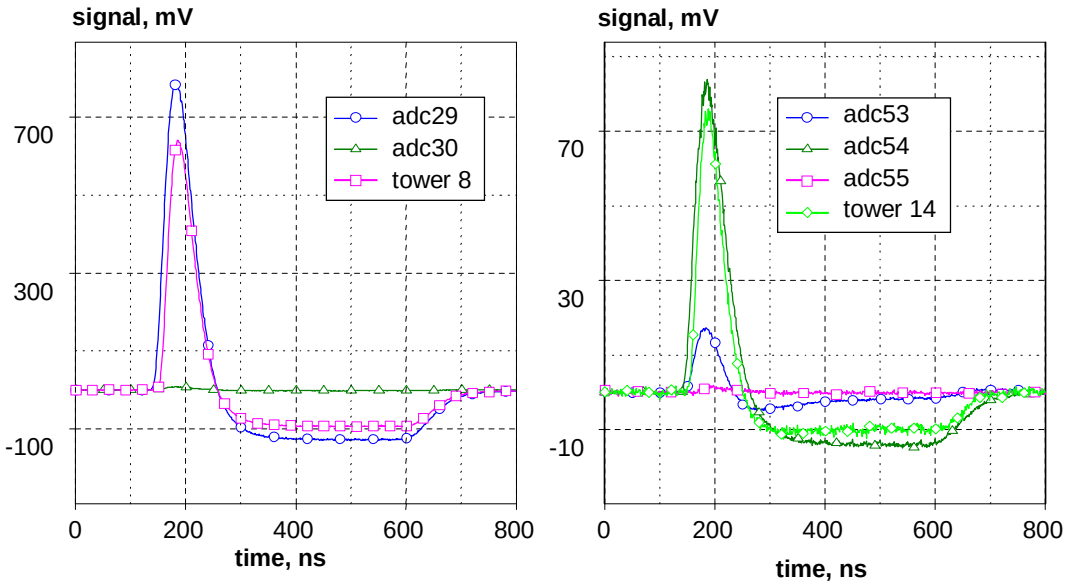


Figure 31: *Ionization signals in the trigger tower 8 and corresponding readout cells (left plot), energy and crosstalk leakage (right plot).*

3.6 Radiation tests

The tower driver board will be placed in the end-cap front-end crate, so the components of the board have to satisfy the ATLAS Radiation Hardness Assurance. The simulated dose and radiation safety factors are summarized in Table 4.

Table 4: *Radiation tolerance criteria for the front-end crate in the end-cap region.*

	Simulated dose	SF sim	SF ldr	SF lot	RTC
γ, Gy	5	3.5	5	4	350
n/cm^2	$1.6\ 10^{11}$	5	1	4	$3.2\ 10^{12}$

There is only one active component on the TDB, the AD8001 fast bipolar operational amplifier produced by Analog Device. These amplifiers have been tested by the Tower Builder Board group and pre-selection tests gave the satisfactory results. The doses achieved in those tests

were 3.2 10^{13} n/cm^2 and 218 Gy for neutrons and γ respectively. The accumulated neutron dose is much higher than needed for the TDB. The γ dose is less than radiation tolerance criteria but close to that. Other components used on the board are chip resistors and ceramic capacitors with known radiation hardness. That is why the special radiation tests of the TDB were not done and we consider that such tests are not needed or they can be done later.

3.7 Burn-in tests

The burn-in tests have not been done with prototype board. This test with one of the full size prototype board is planned for the fall of 2002. Since the board is made of standard components, we do not expect any problems. During the series production, the burn-in will be made by the supplier.

4. TDB production schedule

4.1 Production volume and plans

There are two tower driver boards per each HEC quadrant that leads to 16 TDB for both HEC wheels. In addition 4 boards are needed for FCAL. Two spare boards for the HEC and one for FCAL will be produced. The total production volume will be 23 boards.

The PRR for the tower driver is scheduled for the fall of 2002. All the production and quality assurance tests will be performed in year 2003, so the TDB will be available for installation in year 2004.

4.2 Quality assurance procedure

The quality assurance procedure includes the following five steps:

1. High temperature treatment as the last step of production.
   Each board will be kept at 100° C during 100 hours.
2. Visual inspection. In particular, the accordance of the specified components to the design values has to be checked.
3. DC-tests. The potentials has to be measured in specified points in order to check the working conditions of operational amplifiers, possible shortages and missing connections.
4. Functionality tests.
   All important characteristics have to be measured and compared to a window of acceptable values:
   - Step response measurement and analysis for the time constant and amplification factor
   - Linearity
   - Crosstalk (few channels from each board)
   - Noise.
5. Boards, which do not pass the tests, will be rejected.

Setup for the functionality tests has been developed and used to measure the full size TDB prototype. It is schematically shown on Figure 32. Rectangular pulse generator produces input pulse, which goes to two channels through passive splitter. Four output signals of two channels are digitized by oscilloscope and data read out by PC through GPIB bus. The control program is realized using TESTPOINT software. The special fitting program reconstructs the TDB parameters (G_{TD} and τ_{TD}) from the output waveforms.

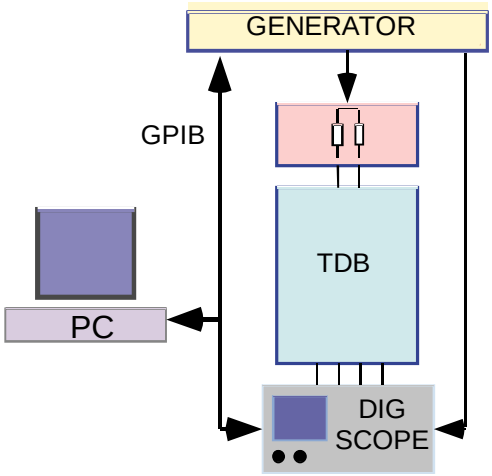


Figure 32: *Setup for the TDB functional tests*

One cycle of measurements takes about 5 minutes mainly due to the linearity ramp. The full board test takes at least 4 hours. So, the quality control of the full production batch can be done within one working month with a good safety margin.

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