ATLAS

HEC Note-132

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Irradiation Test of QL-chips

for MPI Munich

at Dubna Oct. 2000

(MPIrad1)

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MPIrad1

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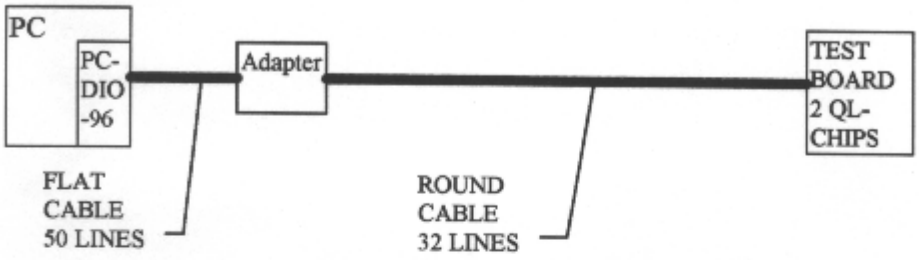
Hardware



Software

It is a running version of a TestPoint program, delivered on a disk and has to be installed under Windows. An input file with test vectors is also on this disk.

Basic SETUP

- Install PC-DIO-96 interface board in a free slot of the PC. In most cases the switch settings of the board will work. In case of problems consult the instruction manual and change settings.
- Switch the PC on.
- Start WINDOWS
- Insert disk „MPIrad1" in drive A: (or B:)
- Select „setup.exe" and double click on left mouse button. The program will be installed at the hard disk „C:\MPIrad1".
- When the program installation is finished, copy the file Qlin.txt from A: (or B:) to C:\MPIrad1\Qlin.txt
- Load the TestPoint program by double click at the icon „MPIrad1". A TP window should appear with an empty table in the lower half and many displays inb the upper half, which are not illuminated.

Test 1: INTERFACE board alone

- In the TP window click „Init". The table should be loaded with the test vectors from the file „Qlin.txt" so that you can read numbers. The round indicators should change to yellow color.
- At the upper right of the TP window you find a small indicator window with the number 10000. Type a small number (2 or 3) in this window and then click the button „Statistics".
- The program should make 2 (or 3) cycles. The displays and the numbers in the table should change from step to step. (Red color means logic 1 and yellow logic 0). At each step an error indication will be shown, because no test object is connected to the interface board.

- You can display the complete error table by clicking on the button „Error report". The table can by saved in the file C:\MPIrad1\Qlerr.txt by clicking „Save List". Rename this file before saving again. Otherwise you will overwrite the old content. You may close the error display table if you like. The content of the action table may be saved in the file C:\MPIrad1\Qlout.txt .by clicking the „Save data" button.

Test 2: INTERFACE board with TESTBOARD

- Connect the test board to the interface by the 50 line flat cable.
- Power (+5V, GND) for the test board are supplied by the interface board.
- Run the TestPoint program as in test 1. No errors should appear.
- Disconnect the test board from 50 line flat cable.

Test 3: FULL CABLING

- Connect the test board and the adapter by the round cable and then connect the flat cable to the adapter.
- Run the test program with a small number of cycles.

FINAL INSTALLATION

- Disconnect the flat cable from the adapter
- Make final mechanical installation of the connected test board at the place close to the reactor, which is foreseen for later irradiation, and put the cable in the final position.
- Connect the flat cable to the adapter.
- Run the test program a few cycles. If there are errors, the reason could be pickup noise on the signal lines. Check shielding and grounding of the cable and try to solve the problem.
- Run the test program for a long time (1 night). No errors should occur.

NOW SYSTEM IS READY FOR IRRADIATION

IRRADIATION

- Run TP-program: „MPIrad1", „Init", „Statistics"
- Measure supply current.
- Start irradiation
- Observe error messages and check supply current after each period of irradiation. It is expected, that radiation damage cause an increase of the error rate and supply current.
- If there are so many errors, that you can conclude the chips are dad, but the supply current is still low, go on with irradiation until the current increases dramatically.
- If current increases dramatically, switch off power immediately and disconnect the flat cable from the adapter. (On the PC-DIO-96 interface board is a 1.5 A fuse in the power line).

MPIrad1

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SCHEMATICS

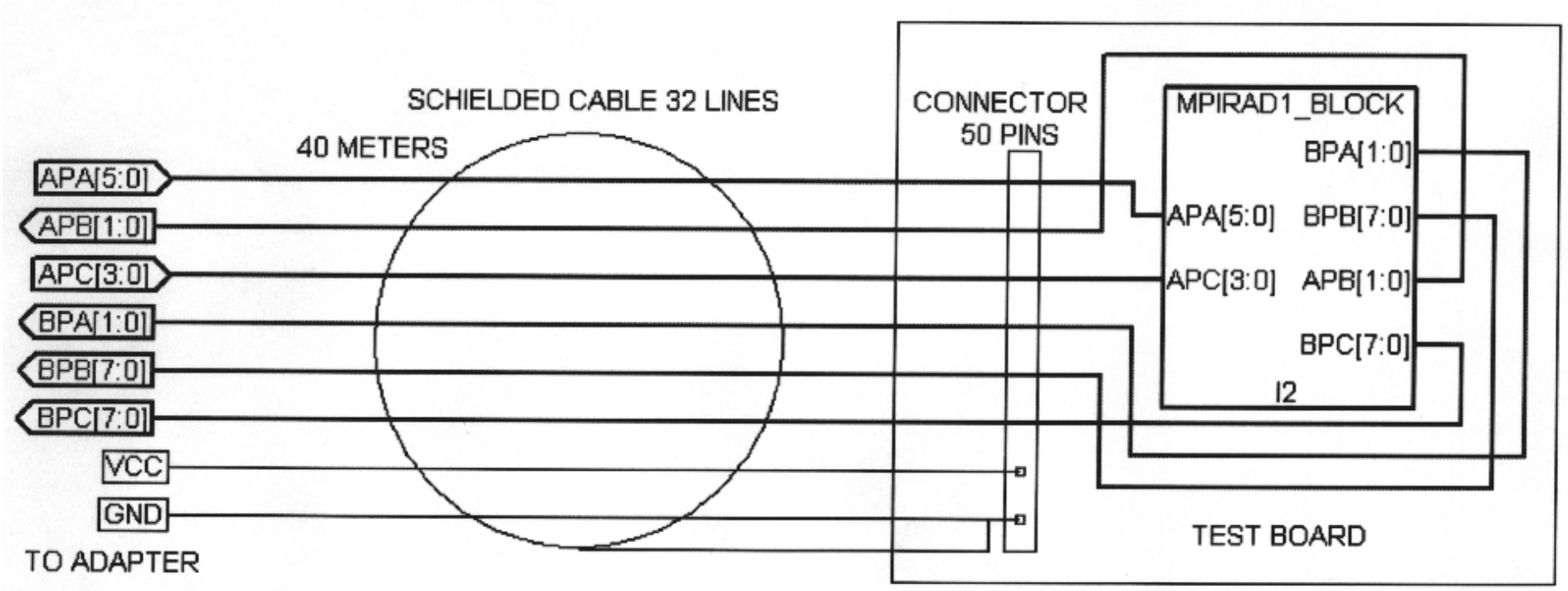
1) Cabling
2) Test board with 2 QL-chips
3) Logic in QL-chip

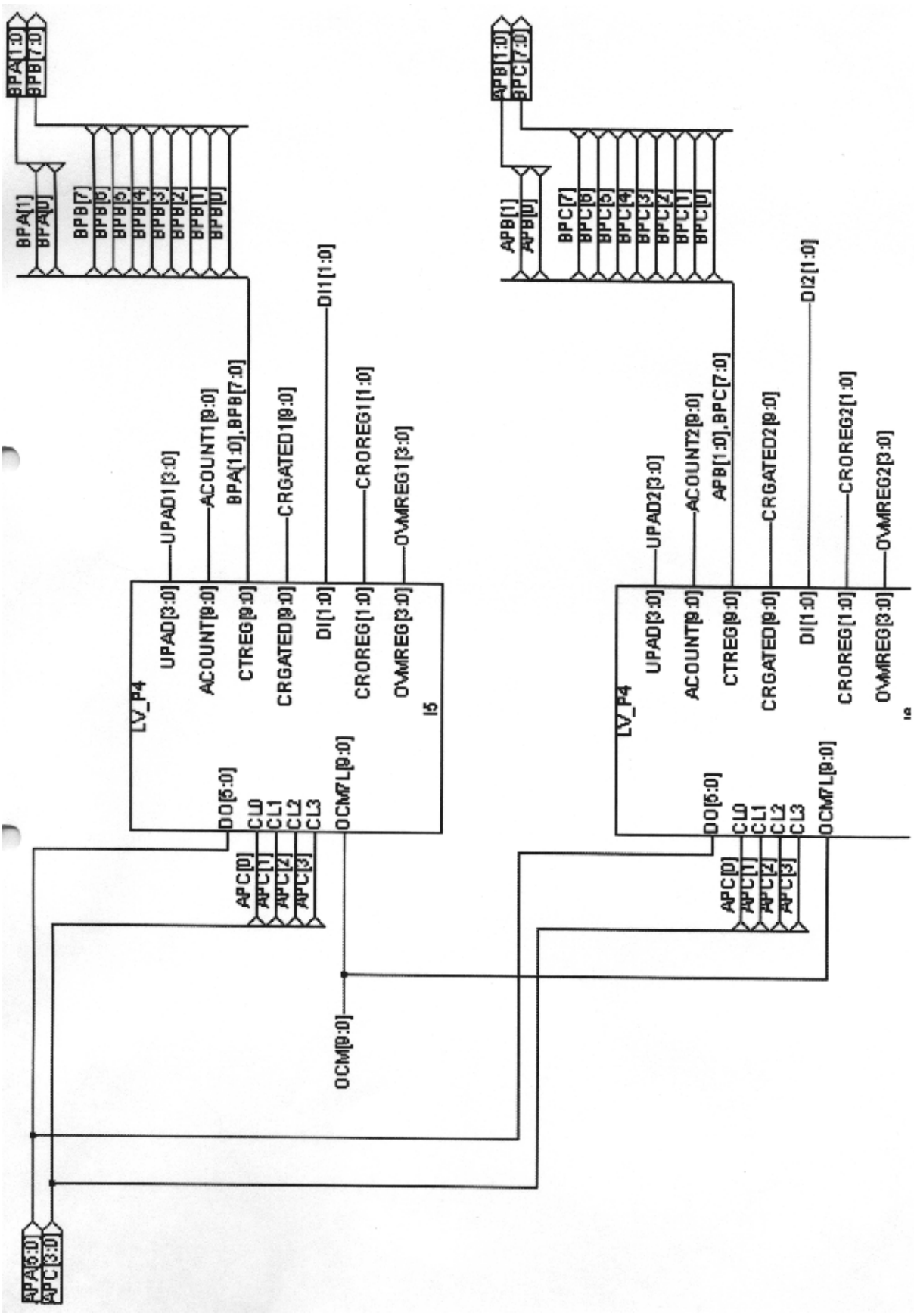
DESCRIPTION OF LOGIC IN THE QL-CHIP

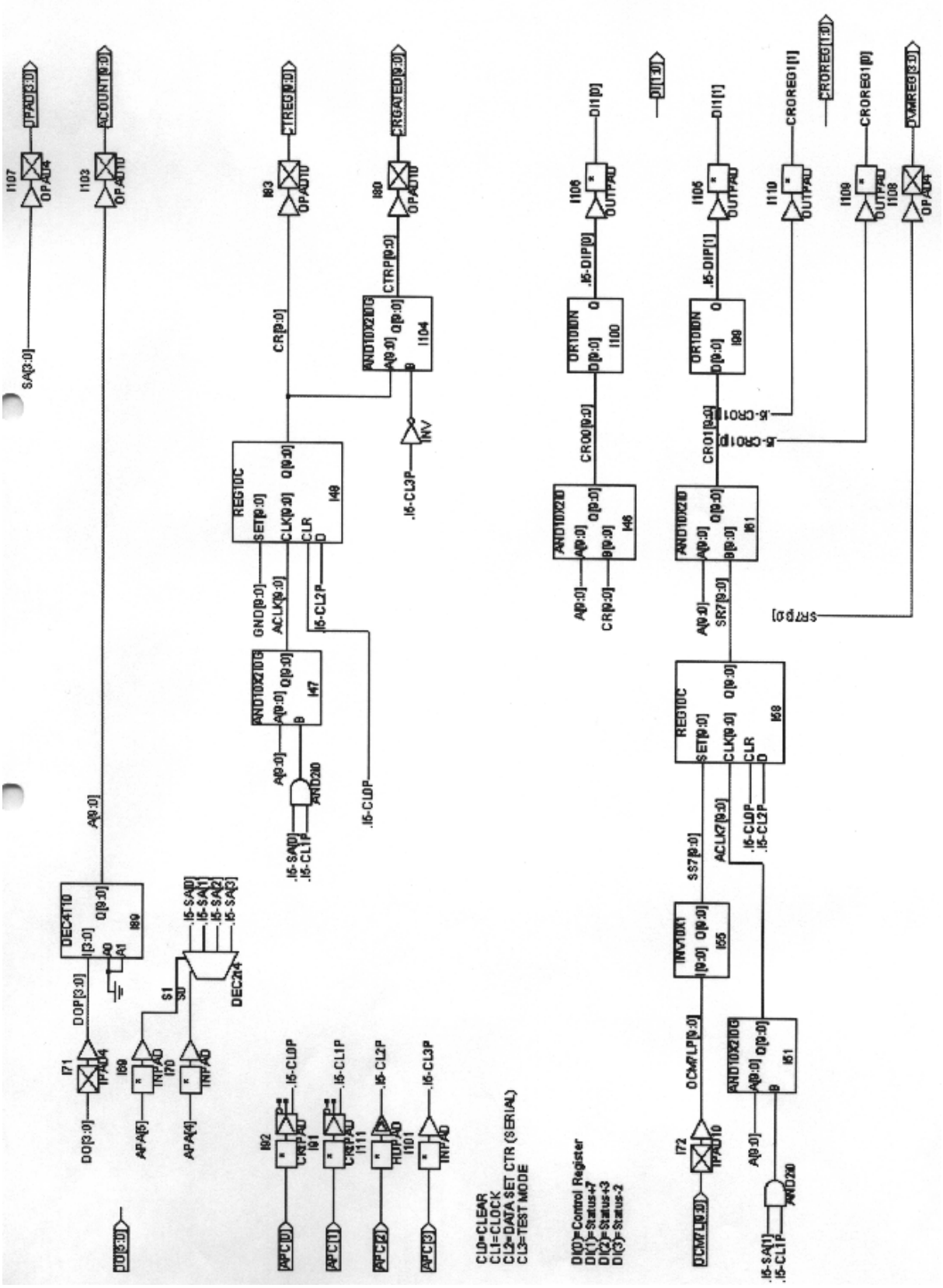
During irradiation only the most important logic blocks operate and are checked by the TestPoint program. (Only their function is described here.)
The decoders DEC4T10 and DEC2T4 decode the number at the 6 address lines APA(5:0). Always 1 output line of DEC4T10 is at logic 1, all the others are logic 0. The output lines of this decoder define which bit of the register REG10C is set when a clock pulse APC(1) arrives.
The register bits are set either to 0 or to 1 depending on the control signal APC(2).
With a reset pulse APC(0) all bits in the register can be set to 0 simultaneously.

TEST PROGRAM

One program cycle consists of 47 clocks (or steps). At the first step all registers are cleared. At the following steps the address is increased from 0 to 9 and the register bits 0 to 9 are set to logic 1 one bit after the other. At the TP screen this is indicated by the 10 indicator lights changing from yellow to red. The left column displays chip 1 and the right column chip 2.
Then the register is cleared and all lights change to yellow. During the next steps the addresses are varied from 16 to 24 and no register bit must be set. All indicators stay at yellow until the end of the complete program cycle.
After each step all input and output signals are written into the action table. If errors occur, the information is written into the error table.


SCHIELDED CABLE 32 LINES
40 METERS
CONNECTOR
50 PINS
MPIRAD1_BLOCK
APA[5:0]
APB[1:0]
APC[3:0]
BPA[1:0]
BPB[7:0]
BPC[7:0]
VCC
GND
TO ADAPTER
APA[5:0]
APC[3:0]
BPA[1:0]
BPB[7:0]
APB[1:0]
BPC[7:0]
I2
TEST BOARD


BPA[1:0]
BPB[7:0]
BPA[1]
BPA[0]
BPB[7]
BPB[6]
BPB[5]
BPB[4]
BPB[3]
BPB[2]
BPB[1]
BPB[0]
APB[1:0]
BPC[7:0]
APB[1]
APB[0]
BPC[7]
BPC[6]
BPC[5]
BPC[4]
BPC[3]
BPC[2]
BPC[1]
BPC[0]
LV_P4
UPAD[3:0]
ACOUNT[9:0]
CTREG[9:0]
CRGATED[9:0]
DI[1:0]
CROREG[1:0]
OVMREG[3:0]
DO[5:0]
CL0
CL1
CL2
CL3
OCMFL[9:0]
I5
UPAD1[3:0]
ACOUNT1[9:0]
BPA[1:0],BPB[7:0]
CRGATED1[9:0]
DI1[1:0]
CROREG1[1:0]
OVMREG1[3:0]
UPAD2[3:0]
ACOUNT2[9:0]
APB[1:0],BPC[7:0]
CRGATED2[9:0]
DI2[1:0]
CROREG2[1:0]
OVMREG2[3:0]
APC[0]
APC[1]
APC[2]
APC[3]
OCM[9:0]
APA[6:0]
APC[3:0]


DO[3:0]
APA[5]
APA[4]
APC[0]
APC[1]
APC[2]
APC[3]
I5-CL0P
I5-CL1P
I5-CL2P
I5-CL3P
I5-SA[0]
I5-SA[1]
I5-SA[2]
I5-SA[3]
DEC4T10
DEC2t4
REG10C
AND10X2
INV10X1
OR10D0N
CLR0=CLEAR
CLI=CLOCK
CL2=DATA SET CTR (SERIAL)
CL3=TEST MODE
DI(0)=Control Register
DI(1)=Status+7
DI(2)=Status+3
DI(3)=Status+2


QuickLogic
pASIC
QL3012-2PL84C
DPB6
APC1