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Tower Driver Board for the ATLAS Hadronic End-Cap and Forward Calorimeters

Production Readiness Review

E. Ladygin

Joint Institute for Nuclear Research, Dubna, Russia

L. Kurchaninov

Max-Planck-Institut für Physik, Munich, Germany

Abstract. This Note presents documentation for the Production Readiness Review of the tower driver board (TDB). The HEC trigger towers pattern and signals summing scheme are described. The board specification requirements, mechanical and electrical design are presented. The prototype boards have been extensively tested in the HEC testbeam environment. The pre-production board has also been designed, produced and tested in laboratory conditions. The results of these tests are presented. Finally, the plans of the production and QC tests are proposed.

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1. Introduction

1.1. TDB design review and follow-up

The tower driver board for ATLAS HEC and FCal calorimeters has been originally designed in year 2001. Two full-scale prototypes have been produced, tested in lab and in HEC testbeam environment, and reviewed in June 2002. The design review document (DR) can be found in CERN EDMS [1]. The board design has been approved with the following comments:

- Voltages on the power lines of the LARG front-end crate fixed to +7.0V (line 4) and -7.0V (line 9). The TDB has to be modified to use these values.
- All power inputs are to be fused, with large safety factors (at least a factor of 2) for the current limits. The fuse should be soldered to the board.
- The usage of voltage regulators is required in all front-end boards. In particular, the TDB circuits biased with +5.2V and -5.2V produced from external +7.0V and -7.0V respectively.
- The TDB will not employ a cooling plate in order to have adequate room on the front panel for the six cable connectors. The resulting off-loading of power to neighbouring boards in the crate has to be measured.
- The Level 1 trigger cables have line impedance of 88Ω , this value should be used when considering resistance values for back termination of the cable.
- The wiring of grounds in TDB should follow the scheme used in tower builder board.
- To study saturation waveforms to insure that there are no surprises.
- Although the pre-selection tests for the AD8001 have been made, ATLAS rules require that radiation tests have to be carried out for the batch of chips used in production.
- It would be prudent to verify that there are no high-frequency oscillations by measuring the spectrum up to 1GHz with a spectrum analyzer.
- Connector shields must be installed (i.e. the holes provided for this installation). This
 is essential to preserve electromechanical integrity of the Front End Crate, by
 providing balanced forces on the spring contact for adjacent boards.

As a follow-up of the design review, the prototype boards have been studied in the HEC-specific front-end crate test in February-March 2003 [2]. After the pinout of negative voltage regulator was fixed, the TDB has been re-designed taking into account all other requirements and recommendations. One pre-production board has been produced and tested in laboratory conditions in the fall 2003.

In this Note we do not reproduce all the results presented in [1], but concentrate on the new design and on the results of the recent tests.

1.2. Note organization and layout

The Note is organized in the following way. Section 2 is devoted to the general architecture of the HEC trigger channels and specification requirements to TDB. Section 3 presents the electrical and mechanical design of the board and in Section 4 we concentrate on the recent measurements of two prototype boards done during the HEC specific front-end crate test in the spring 2003. The results of systematic measurements of the pre-production TDB are presented in Section 5. And finally, in Section 6 we outline the production schedule and quality assurance procedure.

2. HEC trigger architecture

2.1. HEC trigger towers

One wheel of the HEC consists of 32 ϕ -wedges, each of them have 24 η , ϕ bins and 4 longitudinal readout segments, shown schematically in Figure 1. The size of bins is $\eta x \phi = 0.1 \times 0.1$ for $\eta < 2.5$ and 0.2x0.2 for high η . So, each wedge has 96 readout cells, 8 of them are empty because of the first low- η bins are not present in the longitudinal segments 3 and 4, and the last high- η bin is not present in segments 2 and 3. The readout channel is formed by analog summation of signals from individual gaps in preamplifying and summing boards, placed on the outer side of the wedge.



GAPS	1-8	9-16	17-24	25-28	29-32	33-36	37-40
BLOCKS	1	2	3	4	5	6	7
SEGMENTS	1		2		3	4	4

Figure 1: Segmentation of a HEC wedge in η -, ϕ - and z- directions

The trigger tower is formed by analog sum of signals from longitudinal segments of the same η , ϕ location. This summing is performed by the Linear Mixer (LM) of the shaper chip [3] in the front-end boards (FEB). In contrary to the case of electromagnetic calorimeters, no further summation of signals is needed for the HEC L1 trigger system. That is why special types of Layer Sum Boards (LSB) are used for the HEC channels [4]. The board, which finally builds trigger towers of the HEC is called, Tower Driver Board since no summation is implied there. The function of this board is to produce differential signals and to drive 70-m trigger cables.

Simulations of the high-energy jets in ATLAS show that the energy deposition in the HEC last longitudinal segment is very low, typically a few % of total energy deposition. In this case the signal to noise ratio is better if to exclude the 4-th segment from the trigger sum. This will be done by the proper programming of the FEB, therefore it does not affect the TDB design.

In the case of the forward calorimeter, the trigger towers are formed by two steps of summing, both in LM and in LSB. Since no further summation is needed, the TDB will be used also for this detector.

The η -bins of the HEC wheel are numbered from 2 to 15 as shown in Figure 2. In the low η -region there are 16 ϕ -bins (A to P) and in the high- η region there are 8 ϕ -bins (A to H). One HEC quadrant (8 wedges) is read out by 6 FEBs placed in one front-end crate [5]. The cable connections are made in such a way that one FEB processes an η -region of 4 ϕ -wedges. Hereafter we number these FEBs from 1 to 6 according to Figure 2. Each FEB delivers 32 trigger signals, so in total there are 192 trigger channels per quadrant. These signals are collected to two TDB, so each board has 96 channels. We number these TDB as 1 and 2 as shown in Figure 2.



Figure 2: η , ϕ regions of the HEC quadrant and corresponding FEB and TDB numbering.

The numbering of the readout channels is organized according to the FEB numbering scheme. The channels of the first half-quadrant (FEB 1, 3, 5) are numbered from 1 to 384 and of the second half (FEB 2, 4, 6) – from 385 to 768. The second part has a structure, equivalent to the first part. The first 4 channels of FEB1 are connected to 4 longitudinal cells of tower A2, the next 4 channels – to tower B2, then C2, D2, A3, B3, and so on. The first 64 FEB channels deal with ϕ -bins A-D and η -bins 2-5, the last 64 channels – with ϕ -bins E-H and the same η -bins. So, the numbering of readout channels has natural periodical structure with groups of 64 channels, presented in Table 1.

Readout channels	164	65128	129192	193256	257320	321384
HEC	A2D5	E2H5	A6D9	E6H9	A10B15	E10D15
towers						
FEB	FEB 1		FEB 3		FEB 5	

Table1: Numbering of readout channels in the HEC half-quadrant.

2.2. TDB specification requirements

The set of specification requirements to the TDB follows from the electrical characteristics of the input and output loads. The mechanical requirements are determined by the design of the frontend crate [6]. The radiation tolerance and reliability issues are common to all boards in the frontend crate. The list of requirements is given below.

- 1. TDB has the same dimensions as other front-end boards: WxLxH=490x409.5x20.3 mm
- 2. Power supply from the front-end crate power bars 4 (+7V) and 9 (-7V) similar to the tower builder board
- 3. Power dissipation is not more then 15W. It allows do not use the cooling plates
- 4. Input impedance is $50\Omega \pm 5\%$
- 5. High frequency band. Integrating pole is not more than 2 ns
- 6. Gain as a ratio of the output differential to input unipolar amplitudes is close to 1 for $\sim 88\Omega$ output load
- 7. Gain variation from channel to channel (RMS) not more than 1%
- 8. Integral nonlinearity less than 1% for the range of amplitudes up to 3V
- 9. Noise level is low enough so that its contribution to the total noise is less than 5%. For typical noise level at the LSB output it leads to $300\mu V$ of the noise RMS at the TDB output
- 10. Crosstalk is not more than 1%
- 11. Output impedance in each line is $44\Omega \pm 5\%$

12. Radiation stability up to γ -dose of 397 Gy and neutron fluence of 2.9 $\cdot 10^{12}$ n/cm²

Since the power consumption is expected to be very low, the cooling plates are not required. To provide the electromagnetic shielding of the TDB module, the simple aluminium sheets will be used. The TDB is completely analog board, no FPGAs are used, and therefore, both SPAC bus and TTC lines will not be used.

3. TDB design

3.1. Board layout

The board layout is schematically shown in Figure 3. TDB contains 96 channels with elements placed on one side of PCB. All channels are located near the input connectors J1-J3 in order to minimize the length of the signal transmission from FEB. Six output connectors J4-J9 are fixed on the front panel, which is screwed to the PCB via aluminium supports. Fuses, voltage regulators and filters are placed near the power connector. Figure 4 shows a general view of TDB covered with side aluminium sheet, protecting electronics components.



Figure 3: Layout of the TDB. View from the element side.



Figure 4: General view of TDB with side shield installed.

TDB channels are numbered from 0 to 95, the correspondence between channel number and pins of input and output connectors are presented in Tab.2. The PCB has 6 layers with cross section and dimensions shown in [1].

3.2. Channel scheme

The main function of TDB is to transform the unipolar signal coming from LSB to the differential signal and to drive the 70 m twisted pair cable. All signal lines on the baseplane and on the FEB have 50Ω wave impedance. The LSB is designed with the 50Ω output serial resistor in order to achieve approximately the 50Ω output impedance. This allows a high input impedance of the signal receiver since the reflections are damped by the LSB output. Nevertheless the double termination is more effective, therefore a 50Ω input receiver is preferable to reduce both the effects of reflections and input crosstalk.

The TDB channel is schematically shown on Figure 5. It is made by using a high frequency low power amplifier circuit AD8001 [7]. This circuit is chosen because it is used in the tower builder board and all pre-selection tests and production batch qualification have been already made. All resistors and capacitors are standard ceramic SMD parts. No decoupling capacitors are planned both in the input and output stages. The output serial resistors of 43Ω are introduced to protect amplifiers against shorts and to ensure double termination of the output cable.

IDB cn	J1 pin	J4 ch	TDB ch	J2 pin	J6 ch	TDB ch	J3 pin	J8 ch
0	31	0	32	1	0	64	1	0
1	29	1	33	3	1	65	3	1
2	27	2	34	5	2	66	5	2
3	25	3	35	7	3	67	7	3
4	23	4	36	17	4	68	17	4
5	21	5	37	19	5	69	19	5
6	19	6	38	21	6	70	21	6
7	17	7	39	23	7	71	23	7
8	66	8	40	66	8	72	66	8
9	68	9	41	68	9	73	68	9
10	70	10	42	70	10	74	70	10
11	72	11	43	72	11	75	72	11
12	74	12	44	82	12	76	82	12
13	76	13	45	84	13	77	84	13
14	78	14	46	86	14	78	86	14
15	80	15	47	88	15	79	88	15
10	00	15	.,	00	10	17	00	10
TDB ch	J1 pin	J5 ch	TDB ch	J2 pin	J7 ch	TDB ch	J3 pin	J9 ch
TDB ch 16	J1 pin 15	J5 ch 0	TDB ch 48	J2 pin 9	J7 ch	TDB ch 80	J3 pin 9	J9 ch
TDB ch 16 17	J1 pin 15 13	J5 ch 0 1	TDB ch 48 49	J2 pin 9 11	J7 ch 0 1	TDB ch 80 81	J3 pin 9 11	J9 ch 0 1
TDB ch 16 17 18	J1 pin 15 13 11	J5 ch 0 1 2	TDB ch 48 49 50	J2 pin 9 11 13	J7 ch 0 1 2	TDB ch 80 81 82	J3 pin 9 11 13	J9 ch 0 1 2
TDB ch 16 17 18 19	J1 pin 15 13 11 9	J5 ch 0 1 2 3	TDB ch 48 49 50 51	J2 pin 9 11 13 15	J7 ch 0 1 2 3	TDB ch 80 81 82 83	J3 pin 9 11 13 15	J9 ch 0 1 2 3
TDB ch 16 17 18 19 20	J1 pin 15 13 11 9 7	J5 ch 0 1 2 3 4	TDB ch 48 49 50 51 52	J2 pin 9 11 13 15 25	J7 ch 0 1 2 3 4	TDB ch 80 81 82 83 84	J3 pin 9 11 13 15 25	J9 ch 0 1 2 3 4
TDB ch 16 17 18 19 20 21	J1 pin 15 13 11 9 7 5	J5 ch 0 1 2 3 4 5	TDB ch 48 49 50 51 52 53	J2 pin 9 11 13 15 25 27	J7 ch 0 1 2 3 4 5	TDB ch 80 81 82 83 84 85	J3 pin 9 11 13 15 25 27	J9 ch 0 1 2 3 4 5
TDB ch 16 17 18 19 20 21 22	J1 pin 15 13 11 9 7 5 3	J5 ch 0 1 2 3 4 5 6	TDB ch 48 49 50 51 52 53 54	J2 pin 9 11 13 15 25 27 29	J7 ch 0 1 2 3 4 5 6	TDB ch 80 81 82 83 84 85 86	J3 pin 9 11 13 15 25 27 29	J9 ch 0 1 2 3 4 5 6
TDB ch 16 17 18 19 20 21 22 23	J1 pin 15 13 11 9 7 5 3 1	J5 ch 0 1 2 3 4 5 6 7	TDB ch 48 49 50 51 52 53 54 55	J2 pin 9 11 13 15 25 27 29 31	J7 ch 0 1 2 3 4 5 6 7	TDB ch 80 81 82 83 84 85 86 87	J3 pin 9 11 13 15 25 27 29 31	J9 ch 0 1 2 3 4 5 6 7
TDB ch 16 17 18 19 20 21 22 23 24	J1 pin 15 13 11 9 7 5 3 1 96	J5 ch 0 1 2 3 4 5 6 7 8	TDB ch 48 49 50 51 52 53 54 55 56	J2 pin 9 11 13 15 25 27 29 31 74	J7 ch 0 1 2 3 4 5 6 7 8	TDB ch 80 81 82 83 84 85 86 87 88	J3 pin 9 11 13 15 25 27 29 31 74	J9 ch 0 1 2 3 4 5 6 7 8
TDB ch 16 17 18 19 20 21 22 23 24 25	J1 pin 15 13 11 9 7 5 3 1 96 94	J5 ch 0 1 2 3 4 5 6 7 8 9	TDB ch 48 49 50 51 52 53 54 55 56 57	J2 pin 9 11 13 15 25 27 29 31 74 76	J7 ch 0 1 2 3 4 5 6 7 8 9	TDB ch 80 81 82 83 84 85 86 87 88 89	J3 pin 9 11 13 15 25 27 29 31 74 76	J9 ch 0 1 2 3 4 5 6 7 8 9
TDB ch 16 17 18 19 20 21 22 23 24 25 26	J1 pin 15 13 11 9 7 5 3 1 96 94 92	J5 ch 0 1 2 3 4 5 6 7 8 9 10	TDB ch 48 49 50 51 52 53 54 55 56 57 58	J2 pin 9 11 13 15 25 27 29 31 74 76 78	J7 ch 0 1 2 3 4 5 6 7 8 9 10	TDB ch 80 81 82 83 84 85 86 87 88 89 90	J3 pin 9 11 13 15 25 27 29 31 74 76 78	J9 ch 0 1 2 3 4 5 6 7 8 9 10
TDB ch 16 17 18 19 20 21 22 23 24 25 26 27	J1 pin 15 13 11 9 7 5 3 1 96 94 92 90	J5 ch 0 1 2 3 4 5 6 7 8 9 10 11	TDB ch 48 49 50 51 52 53 54 55 56 57 58 59	J2 pin 9 11 13 15 25 27 29 31 74 76 78 80	J7 ch 0 1 2 3 4 5 6 7 8 9 10 11	TDB ch 80 81 82 83 84 85 86 87 88 89 90 91	J3 pin 9 11 13 15 25 27 29 31 74 76 78 80 80	J9 ch 0 1 2 3 4 5 6 7 8 9 10 11
TDB ch 16 17 18 19 20 21 22 23 24 25 26 27 28	J1 pin 15 13 11 9 7 5 3 1 96 94 92 90 88	J5 ch 0 1 2 3 4 5 6 7 8 9 10 11 12	TDB ch 48 49 50 51 52 53 54 55 56 57 58 59 60	J2 pin 9 11 13 15 25 27 29 31 74 76 78 80 90	J7 ch 0 1 2 3 4 5 6 7 8 9 10 11 12	TDB ch 80 81 82 83 84 85 86 87 88 89 90 91 92	J3 pin 9 11 13 15 25 27 29 31 74 76 78 80 90	J9 ch 0 1 2 3 4 5 6 7 8 9 10 11 12
TDB ch 16 17 18 19 20 21 22 23 24 25 26 27 28 29	J1 pin 15 13 11 9 7 5 3 1 96 94 92 90 88 86	J5 ch 0 1 2 3 4 5 6 7 8 9 10 11 12 13	TDB ch 48 49 50 51 52 53 54 55 56 57 58 59 60 61	J2 pin 9 11 13 15 25 27 29 31 74 76 78 80 90 92	J7 ch 0 1 2 3 4 5 6 7 8 9 10 11 12 13	TDB ch 80 81 82 83 84 85 86 87 88 89 90 91 92 93	J3 pin 9 11 13 15 25 27 29 31 74 76 78 80 90 92	J9 ch 0 1 2 3 4 5 6 7 8 9 10 11 12 13
TDB ch 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30	J1 pin 15 13 11 9 7 5 3 1 96 94 92 90 88 86 84	J5 ch 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14	TDB ch 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62	J2 pin 9 11 13 15 25 27 29 31 74 76 78 80 90 92 94	J7 ch 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14	TDB ch 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94	J3 pin 9 11 13 15 25 27 29 31 74 76 78 80 90 92 94	J9 ch 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14

Table 2: TDB channels and corresponding pins of input and output connectors.

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Figure 5: TDB channel scheme.

3.3. Grounding

There are several constraints to the grounding of boards in the FEC [6]. The crate baseplane has common ground, connected to ground pins of the input connectors, special "power" plugs, installed near each side connector, and to the connector spring contacts. Like all the front-end boards, the TDB ground is connected to the baseplane common ground through these three points. Therefore, TDB will be equipped with "power" pins and shields, covering input connector. There are also 64 ground pins in each of three input connectors J1-J3. These parts are not present in the pre-production board.

The output ground connections are organized in the same way as in the tower builder board (see [8], Fig.39). The front panel is connected to PCB ground layers via metal supports (see Section 3.5). The trigger cable has five ground shields – the global shield and four individual shields of twisted pairs [9]. Both grounds are connected to special pins of the cable connector as shown on Figure 6. The corresponding pins of the TDB output connectors are soldered to the PCB ground layer. In addition, the cable global shield is connected to the connector cover, which gives additional ground contact to the front panel.



Figure 6: TDB output connector. Special pins are assigned for global and local shields.

The TDB analog ground is realized at all of six PCB layers, it occupies all space, which is free of signal and power lines.

3.4. Power distribution

The consuming power is very important for the TDB since the usage of standard cooling plates is problematic. Practically all the front panel space is occupied by the output connectors so, there is not enough room for the water plugs. A small heat, produced by TDB will be taken out by the cooling plates of the neighbouring front-end boards.

The TDB power consumption can be easily estimated by using specification data of the amplifier circuit. The consuming current is 5.5mA for bias voltages of \pm 5.2V and therefore all 192 amplifiers of the TDB require 1.06A from both power lines. The total dissipating power of amplifiers is 11.02W and it is distributed over the big area of board. In order to protect the voltage regulators from overheating, the special foam is using to contact them thermally to the aluminium side shield. The total dissipating power including regulators is 14.8W. No warming is expected under these conditions, so a special cooling is not needed, that was confirmed by dedicated tests (see Section 4.2).

The low voltage distribution of TDB is shown on Fig.7. The inputs are protected by 3A fuses soldered near the connector. The required bias of the TDB channels of +5.2V and -5.2V is produced by using radiation-hard voltage regulators LHC4913 (positive) and LHC7913 (negative). The pre-production TDB is equipped with an obsolete version (JQ5) of LHC7913 because the final version was not available when TDB had been assembled. Two independent channels have been selected in order to increase the safety factor of board and decrease the power dissipation of a single voltage regulator. Each operational amplifier has the power filter composed of 10 Ω resistor and 0.47µF ceramic capacitor. The layout of low voltage components is shown on Figure 8.



Figure 7: TDB low voltage distribution scheme.



Figure 8: Low voltage circuits of TDB.

3.5. Front panel and side shield

According to the general rules of RF shielding, the front panel is connected to the FEC mass through screws and completes the Faraday cage. The connection of the front panel to the board ground is provided through the aluminium support brackets and additionally for the reliable electrical contact, the special short wires will be soldered to PCB and screwed to connector nuts.

For the TDB we use LARG standard front-end panel equipped with side spring gaskets. The holes for screws and connectors are made according to the drawing shown on Figure 9.



Figure 9: Layout of holes at the TDB front panel.

The element side of TDB is covered by aluminium shield (see Figure 10) for mechanical protection of components and to conduct the heat from voltage regulators. Thermal contact between voltage regulator packages and shield is provided by special thermal contact foam of the similar type as used in FEB.



Figure 10: TDB side protection shield.

4. Tests of prototype boards

4.1. HEC FEC tests in 2003

The tests of the HEC half-crate have been carried out within the common LARG-wide activity for validation of the front-end electronics [2]. The tests have been performed in the HEC testbeam environment in CERN SPS North Area with using 3 Module-0 front-end boards equipped with final versions of preshapers, shapers and LSBs. Two prototype TDBs are connected to L1 receiver boards with 70-m L1 trigger cables. The trigger signals are read out by a commercial digitizer. In parallel, the FEB output data are acquired by readout drivers (not shown in Figure 11). In addition, the waveforms have been taken by digital oscilloscope.

Some of the measurements have been dedicated to qualify the tower driver board in the realistic conditions. The main results of these measurements are presented below.



Figure 11: HEC specific front-end crate test setup.

4.2. Temperature conditions

The temperature variations in the crate have been studied with nominal positions of TDB1 and two neighbouring FEB2 and FEB3. Two temperature sensors of each FEB have bean read out each 12 seconds during two hours. The temperature readings of stand-alone reference FEB6 have

been subtracted in order to exclude the ambient effects. During the measurements all FEBs were powered on but no triggers generated in the system, so no signal processing performed by FEBs and by TDB.

Figure 12 shows the temperature variations measured by four temperature probes. The measuring cycle started when TDB was powered on. After some 35 minutes the TDB was disconnected from low voltage bus and measurements continued during next half hour. Afterwards the TDB was powered on again.

It can be seen that there is practically no effect of TDB heating on the boards in neighbouring slots. Very small temperature variation, correlated with TDB powering, can be observed at the level of measurement accuracy. From here one can conclude that the TDB does not affect the heating conditions in the front-end crate.



Figure 12: Temperature at front-end boards placed near the TDB.

4.3. Signals saturation

The signal waveforms have been taken by applying calibration signal of different amplitudes (DAC settings in calibration board) and delay. The left plot of Figure 13 shows raw waveforms at ADC level. The digitizer chain as well as all other parts of the full trigger chain have been carefully calibrated and parameterized including attenuation in adapter (block APP in Figure 11) and distortion in coaxial cables. The APP attenuation is mostly responsible for the significant difference of signal amplitudes at the ADC level and at the Receiver output. The chain calibration makes it possible to de-convolute shapes to any point of the trigger chain and to identify, where the saturation comes from. Such a prediction is presented on the right plot of Figure 13. In this particular measurement the signal is saturated in LSB at amplitude of about 3.0V. This value is less than expected for final FEB due to lower LSB bias voltages used in the Module-0 FEB.



Figure 13: Signal waveforms at ADC level (left) and reconstruction of amplitudes at FEB output level (right).

4.4. Amplitude vs. pseudorapidity

The amplification factors of trigger channels have to be chosen from the condition that amplitudes for $E_T = 256 \text{GeV}$ are between 1250mV and 2500mV in order to fit the range of receiver gain adjustment. Detailed waveform studies made for the HEC trigger chain allow to parameterize all parts and to predict the trigger signal shape and its amplitude for ATLAS conditions.

Figure14 (left plot) shows the receiver output amplitudes calculated for $E_T = 256$ GeV. The gains of LM and of LSB are selected to minimize the spread between different η -bins. The last η -bin produces low signal because a significant part of energy is deposited in FCAL. This part is not added to the corresponding trigger channel.

The receiver gain will be chosen from the condition of the equal E_T response for all towers. The gain factors required for receiver channels are also presented on Figure 14 (right plot). It is seen that all gains are within specification window 1.0 - 2.0.



Figure 14: Predicted amplitudes (left) and calculated gain of corresponding receiver channels (right).

5. Tests of pre-production board

5.1. Functional tests

The pre-production TDB functionality has been evaluated in laboratory conditions. The gain and integration time constant were determined by measuring step response, applying the signal from rectangular pulse generator. The input and output signals are measured simultaneously. The function is parameterized by integration pole (rise time τ_{TD}) and gain factor G_{TD} . The correction of the gain to ATLAS conditions, taking into account the LSB output serial 50 Ω resistor and TDB serial output resistor 43 Ω , is made off-line.

Distributions of these two parameters measured for 96 channels of TDB are presented on Figure 15. The average gain is very close to its design value of 0.98 and the spread from channel to channel is 0.3% that is much less than the specification requirement (1%). The integration time constant is less than 1 ns for all channels, that is also less than the specified boundary.



Figure 15: Distributions of gain (left) and rise time (right) for 96 channels of TDB.

The crosstalk between neighbouring channels is less than 1% when measured with rectangular input signal.

The linearity range measured for rectangular input signal is shown on Figure 16 (left plot). The typical output voltage swing is about 3.15V. The nonlinearity in the range up to 3.1V is less then 0.1% (right plot).



Figure 16: Typical linearity plot for rectangular input signal (left) and nonlinearity (right).

The TDB response in the saturation range is different from linear transfer function. Figure 17 shows an example of waveforms measured in linear range (LSB out 1.0V - 3.2V) and shape distortion due to saturation effects in operational amplifiers (LSB out 4.0V - 6.0V). The only change in the shape is the increase of its width, no surprising effects are observed.



Figure 17: TDB rectangular pulse response in linear and in saturation range.

5.2. Noise studies

The TDB noise performance has been extensively studied with prototype board both in laboratory conditions and in HEC testbeam setup. No evident excess noise was detected [1, 2]. Nevertheless, the dedicated measurements have been performed with pre-production TDB to study the noise performance in different loading conditions.

It was found that few channels are sensitive to the input load. As show on Figure 18, the typical noise RMS is $100-200\mu$ V that is well within the specification requirements (300μ V). Some excess noise appears at the positive output when the input left unloaded, but the RMS of the most of channels is still below required boundary. Oscillograms for channel 75 are shown on the right plot of Figure 18. Some periodic (~50ns) structure of pedestal can be observed at the positive output of channel when its input is open.



Figure 18: RMS values for 96 *TDB* channels (left) and output noise oscillograms (right) for channel 75.

The noise structure has been also studied with HP 4195 spectrum analyzer (frequency band up to 500 MHz). Figure 19 shows the noise spectrum for positive output of a good channel (left plot). No high frequency oscillations detected, at least up to 500 MHz. The right plot of Figure 19 demonstrates the origin of an excess noise in a "bad" channel (channel 75). The oscillation is good seen in the range of 20 MHz when the input is unloaded.

The behaviour of excess noise has been studied while the serial resistor is added to noninverting input of positive output branch (see Figure 4). The noise RMS and output signal waveform as a function of resistor value is shown on Figure 20. The noise is effectively damped already for small value. At the same time the rise time and amplitude are practically not changed.

In the front-end crate the TDB inputs are loaded by 50Ω serial resistors at LSB outputs, so the appearance of excess noise is not expected in ATLAS. But for a safety margin, a serial resistor of 100Ω will be added to the scheme.



Figure 19: Noise spectrum for typical channel (left) and for noisy channel ch75 (right).



Figure 20: Dependence of noise RMS (left) and waveform of output signal (right) on nominal of input serial resistor.

5.3. Radiation tests

The tower driver board will be placed in the end-cap front-end crate, so the components of the board have to satisfy the ATLAS Radiation Hardness Assurance. The simulated dose and radiation safety factors taken from [10] are summarized in Table 4.

Table 4: Radiation tolerance criteria for the front-end crate in the end-cap region.

	Simulated dose	SF sim	SF ldr	SF lot	RTC
γ, Gy	5.67	3.5	5	4	397
n/cm ²	$1.45 \cdot 10^{11}$	5	1	4	$2.9 \cdot 10^{12}$

There is only one active component on the TDB, the AD8001 fast bipolar operational amplifier produced by Analog Device. These amplifiers have been tested by the Tower Builder Board group [11] and pre-selection tests gave the satisfactory results. The doses achieved in those tests were $3.2 \cdot 10^{13}$ n/cm² and 2180 Gy for neutrons and γ respectively. Both accumulated neutron and γ doses are much higher than needed for the TDB tolerance. Other components used on the board are chip resistors and ceramic capacitors with known radiation hardness. That is why the special radiation tests of the TDB were not done and we consider that such tests are not needed.

6. TDB production schedule

6.1. Production volume and plans

There are two tower driver boards per each HEC quadrant that leads to 16 boards for both HEC wheels. In addition 4 boards are needed for FCAL. Two spare boards for the HEC and one for FCAL will be also produced. The total production volume will be 23 boards.

All the production and quality assurance tests will be performed in year 2004, so the TDB will be available for installation by year 2005. The rough schedule alone with responsibilities of Institutes is presented in Table 5.

	Date	Task	Quantity	Responsibility
1	February-March 2004	Final PCB design		JINR
2	March-September 2004	Production of:		
		- PCB	23	JINR
		- Front panel	23	MPI
		- Side shield	23	MPI
		- Bracket	92	MPI
		- Spacer	299	MPI
3	October-December 2004	QC tests	23	MPI
4	January 2005	Delivery to CERN	23	MPI

Table 5:	Main	steps	of TDB	production.
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6.2. Quality assurance procedure

The quality assurance procedure includes the following steps:

- 1. High temperature treatment as the last step of production. Each board will be kept at 100°C during 100 hours.
- 2. Visual inspection. In particular, the accordance of the specified components to the design values has to be checked.
- 3. DC-tests. The potentials have to be measured in specified points in order to check the working conditions of voltage regulators and operational amplifiers, possible shortages and missing connections.

4. Functionality tests.

All important characteristics have to be measured and compared to a window of acceptable values:

- Time constant and amplification factor
- Linearity
- Crosstalk (few channels from each board)
- Noise

Boards, which do not pass the tests, will be rejected and repaired if possible.

Setup for the functionality tests has been developed and used to evaluate the TDB preproduction board. It is schematically shown on Figure 21. Rectangular pulse generator produces input signal, which goes to two channels through a passive splitter. Four output signals of two channels are digitized by oscilloscope and data read out by PC through GPIB bus. The control program is realized using TESTPOINT software. The special fitting program reconstructs the TDB parameters (G_{TD} and τ_{TD}) from the output waveforms.



Figure 21: Setup for the TDB QC tests.

One cycle of measurements takes about 15 minutes mainly due to the linearity ramp. The full board test takes at least 12 hours. So, the quality control of the full production batch can be done within two working months.

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