LV Power Box
for the HEC Front-end Electronics
(Document for the PRR of the Power Board)

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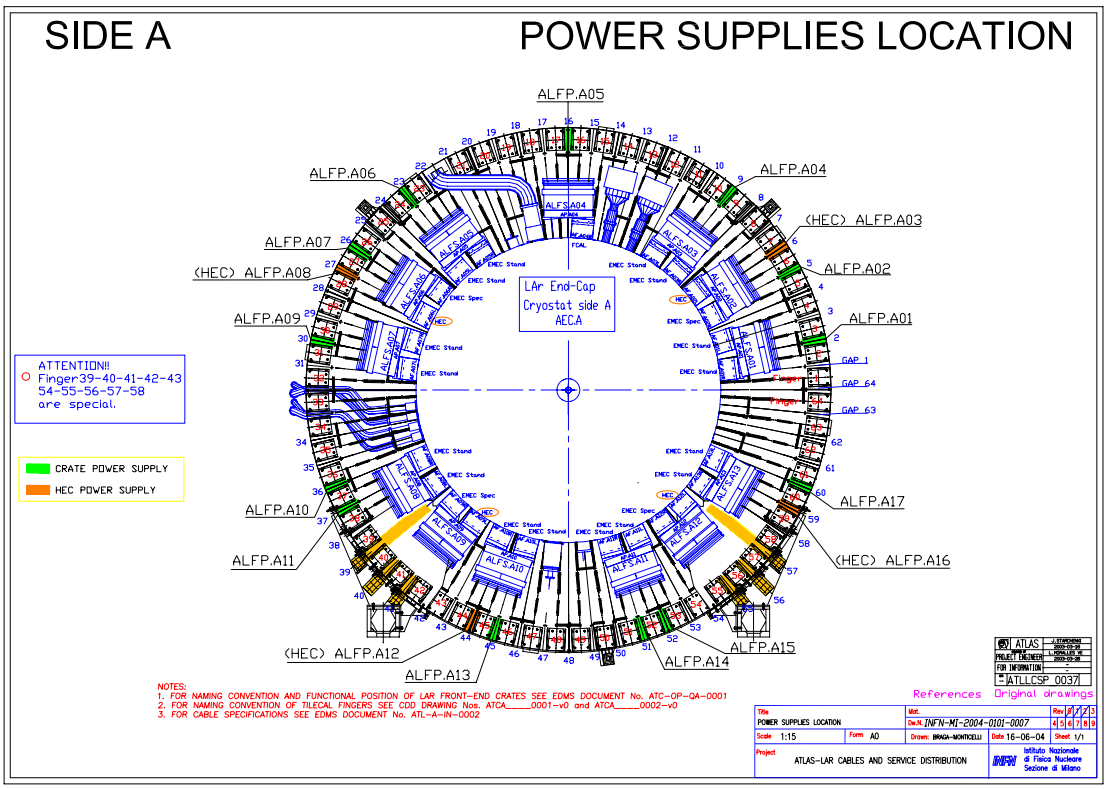
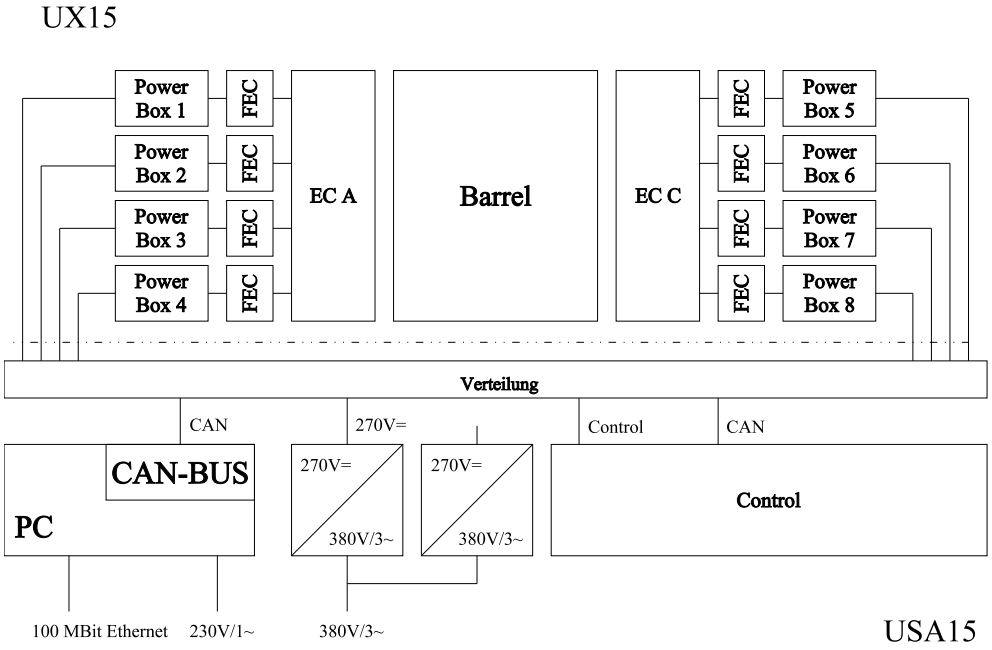
Chapter 1

Overview





1.1 Requirements

The design of the power supply for the preamplifiers of the Hadronic Endcap Calorimeter (HEC) are discussed. The HEC calorimeter is part of the ATLAS detector at CERN. It consists of two end caps. Each end cap has 160 Preamplifier and Summing Boards (PSB). The total sum is 320 PSB‘s.
Voltages for a PSB are:

- 7.0V (7.2V at the output of the Low Voltage - Powerbox (LV-PB))
- 3.0V (3.2V at the output of the LV-PB)
- -1.5V (-1.6V at the output of the LV-PB)

For the power supply it is important to know, that there are different types of PSB Boards.
The maximum currents per PSB for operation in the warm are:

- I(7.0V)= 0.50 A
- I(3.0V)= 0.19 A
- I(-1.5V)= 0.09 A

1.2 Realization

The system consists of different parts.

- conversion from 380V AC to 270V DC
- conversion of the input 270V DC to the three middle Voltages (9V/5V/-3V).
- conversion of the middle voltages to the three output voltages ($7.2\ V/3.2\ V/-1.6\ V$).

1.2.1 Location at detector:

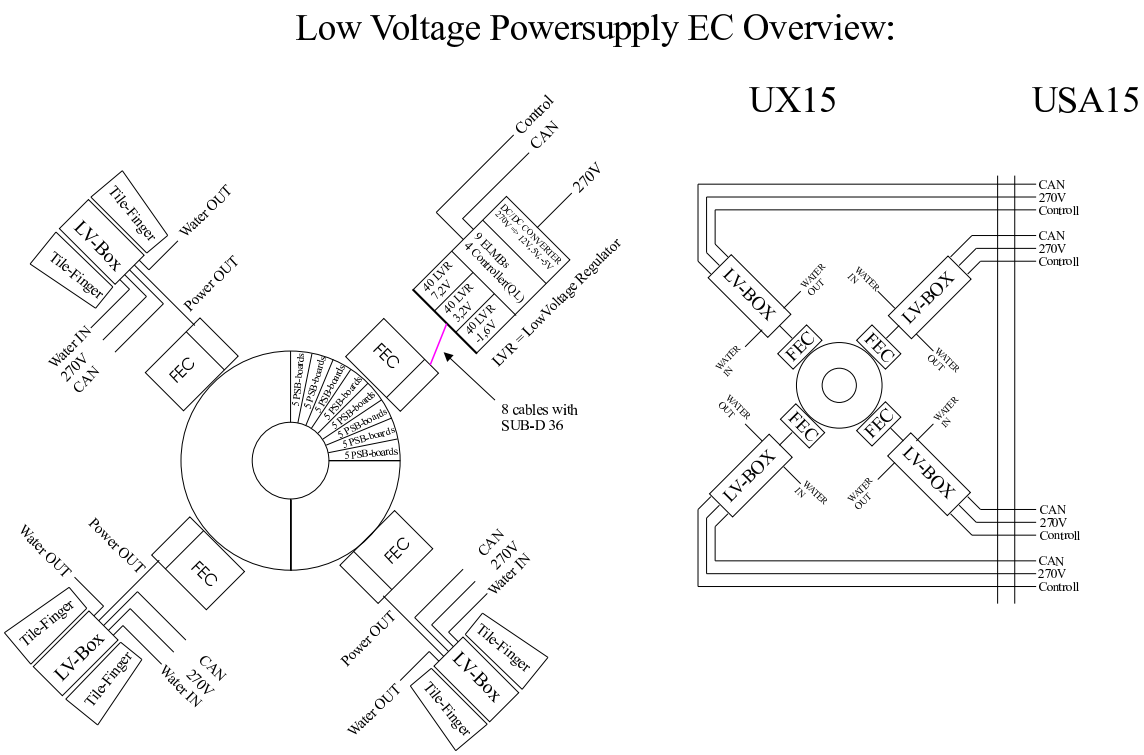


Figure 1.1: Low Voltage Power supply EC overview

The components are at the following locations:

USA15	Conversion of the 380 V AC Voltage to 270 V DC.
TILE-Finger-Region	HEC-Low-Voltage-Power-supply-Box Conversion of the 270 V DC to the three middle Voltages. Conversion of the middle voltages to the output voltages.
FEC(Frond end Crate)	In the Front End Crate are two one inch wideconnection boards connected to the related feed through. The two boards are without active electronic components.
Cryostat	The HEC calorimeters with the PSB boards are located inside the cryostat.

Control and monitor requirements:

- All output channels can be switched on and off separately. One channel consists of three voltages.
- It is possible to measure the current and voltage of each channel and output separately.

- The control and monitoring of the Power Box is done with the SCADA Software PVSS3 from ETM (Austria).

Realization for higher safety requirements:

- For each middle Voltage two redundant DC/DC Converters are located in the Low-Voltage-Power-supply-Box.
- Additional serial interfaces for the control of the power box.

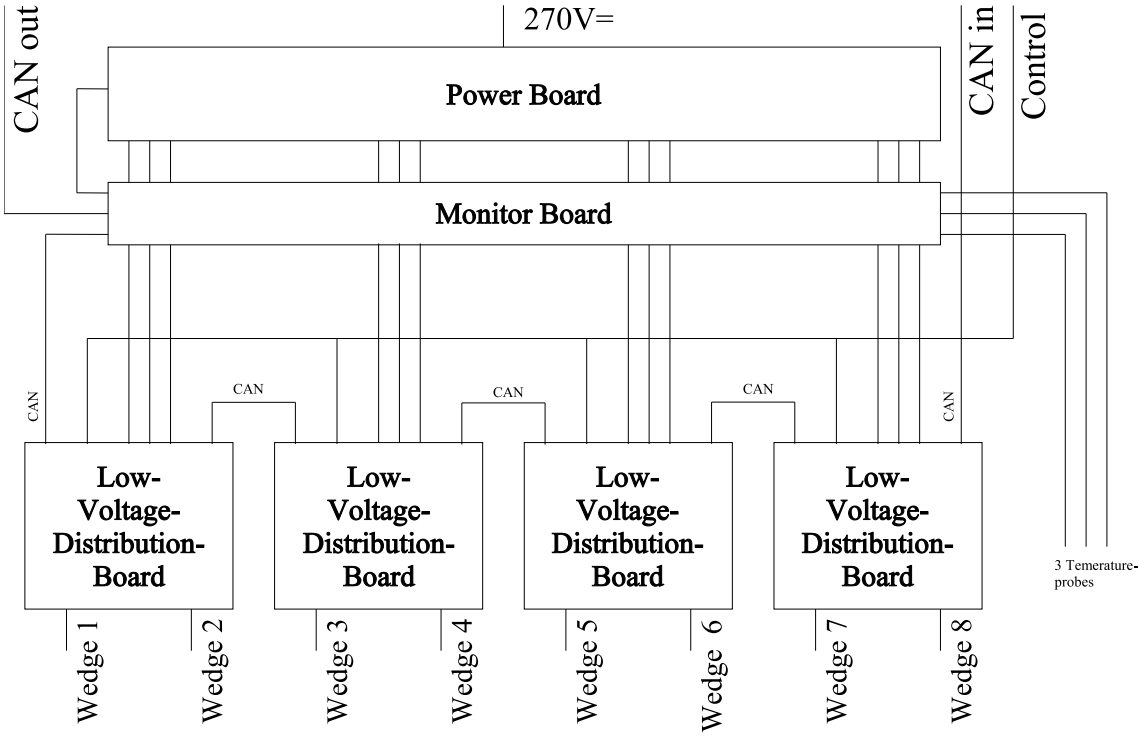
Device overview:

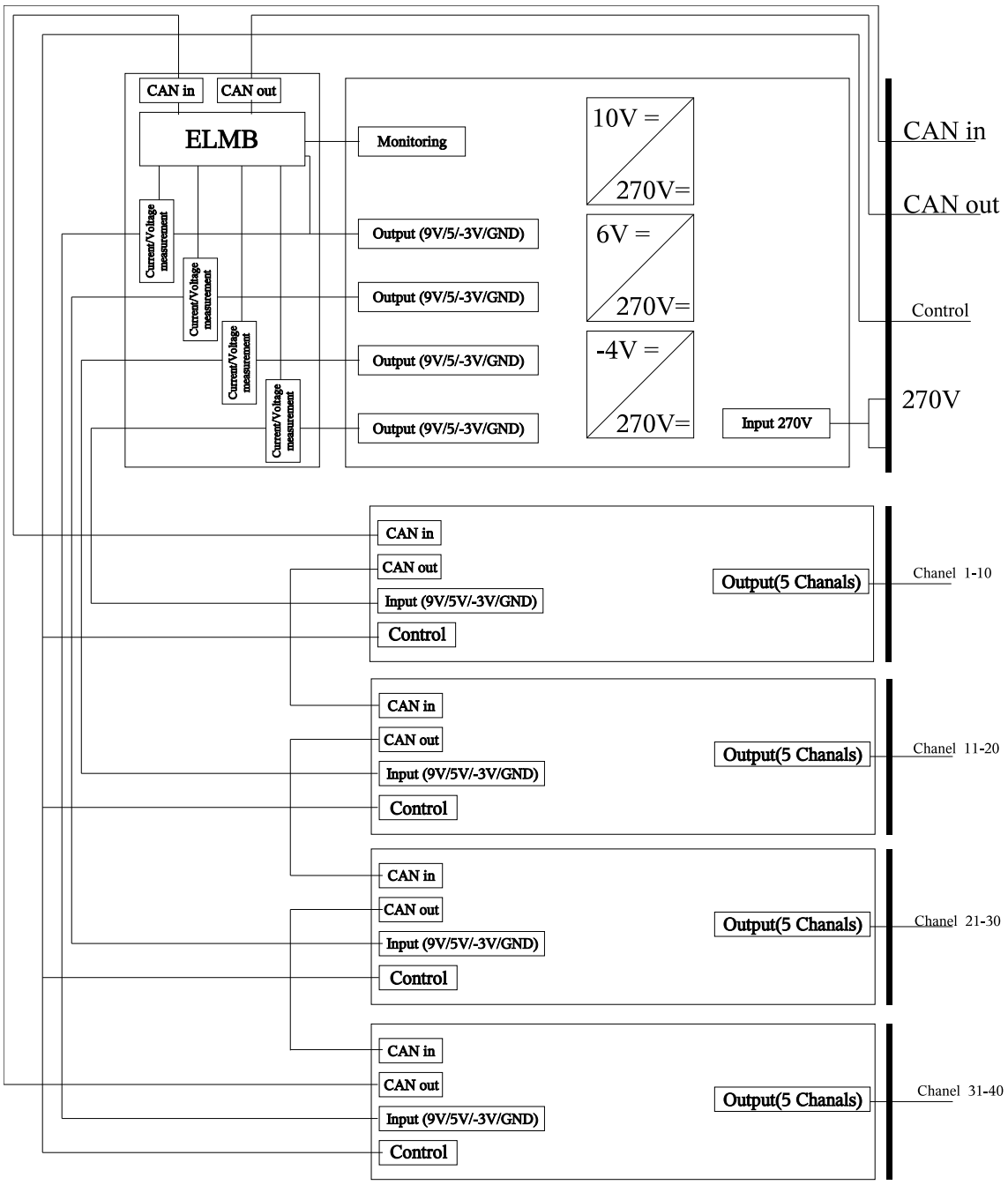
	ELMBs	QL-Chips	PSB boards	Voltage Regulators	
				positive	negative
Low Voltage Supply System for 2 EC	72	32	320	712	320
1 EC(with 4 Quadrants)	36	16	160	356	160
1 Quadrant (power box)	9	4	40	89*	40
1 Wedge(power supply channel	1	0.5	5	10	5
1 channel				2	1

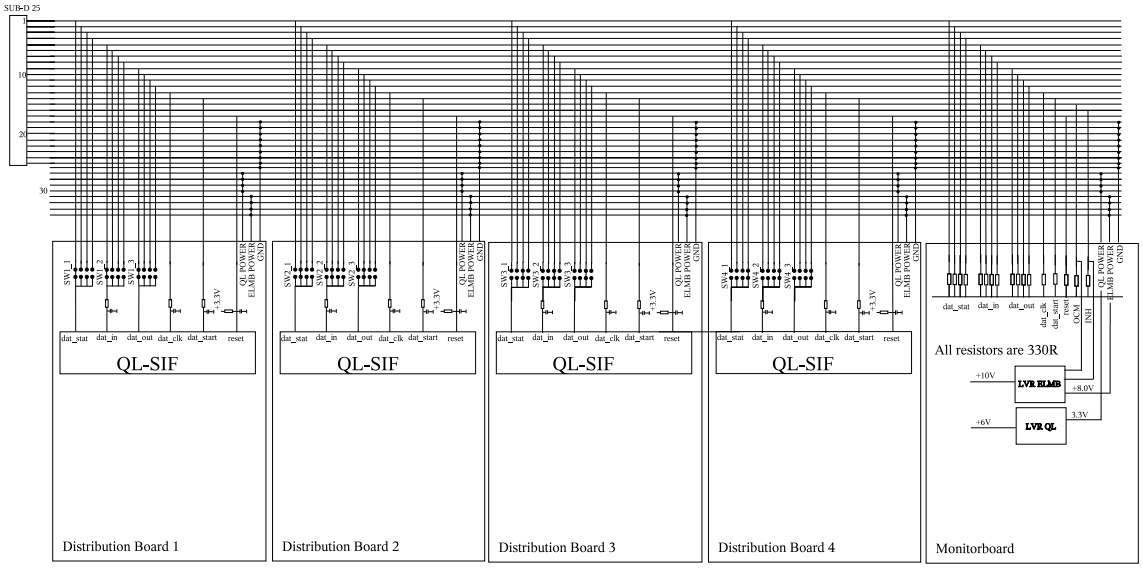
Chapter 2

Power Box

The Power Box consists of 3 layers: the power board, the monitoring board and the distribution boards. The first layer are the converters from 270V DC to the different middle voltages. The Low Voltage Regulators convert the middle voltages to the output voltages and are located on the distribution boards. The Low Voltage Regulators can be switched on and off from the controller chip. The controller chip switches all three Voltages of one channel at once. It gets the status information from each Low Voltage Regulator. This status information shows if there is an overcurrent. The Controller has an interface to the CAN-Bus node (ELMB). The three Voltages and Currents for each PSB Board can be measured separately. Each Box provides the power supply for 40 PSB Boards. Each PSB Board can be switched on and off separately.




CAN in
CAN out
ELMB
Monitoring
10V =
270V=
6V =
270V=
-4V =
270V=
Current/Voltage measurement
Current/Voltage measurement
Current/Voltage measurement
Current/Voltage measurement
Output (9V/5/-3V/GND)
Output (9V/5/-3V/GND)
Output (9V/5/-3V/GND)
Output (9V/5/-3V/GND)
Input 270V
CAN in
CAN out
Control
270V
CAN in
CAN out
Input (9V/5V/-3V/GND)
Control
Output(5 Chanals)
Chanel 1-10
CAN in
CAN out
Input (9V/5V/-3V/GND)
Control
Output(5 Chanals)
Chanel 11-20
CAN in
CAN out
Input (9V/5V/-3V/GND)
Control
Output(5 Chanals)
Chanel 21-30
CAN in
CAN out
Input (9V/5V/-3V/GND)
Control
Output(5 Chanals)
Chanel 31-40



2.1 Power Board (DC/DC converter)

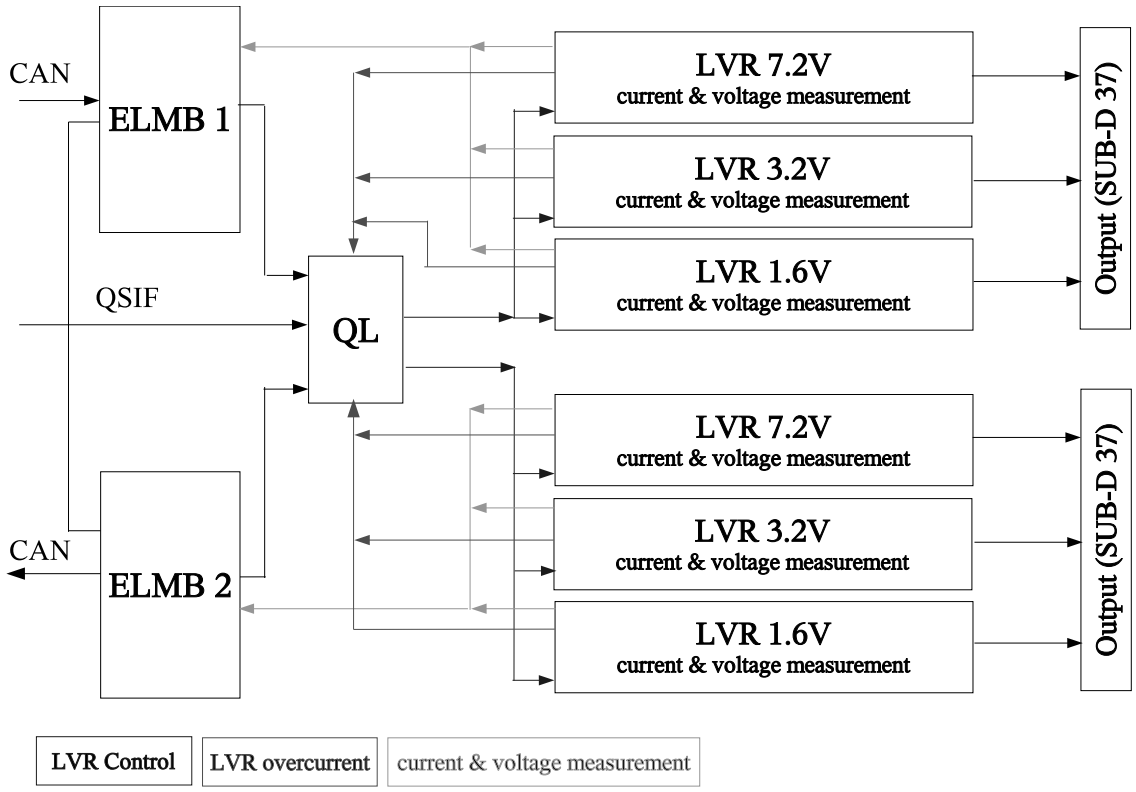
The Power Board converts the 270 Volt DC to the three middle Voltages. The board consists of the DC/DC converter and has a 1+1 safety, which means that one device per Voltage output can be destroyed and the output channel will still work.

2.2 Distribution Board

The Distribution Board consists of two ELMB‘s, one Low Voltage Controller (Quick-Logic chip QL3012-2PF144C), 80 positive Low Voltage Regulators and 40 negative Low Voltage Regulators. The ELMB‘s have an interface to the Low Voltage Controller.

2.2.1 Input voltages, CAN, Control

For the Low Voltage Regulators and the power supply of the ELMB and Quick-Logic Chip we need three input Voltages: 9V, 5V and -3V.



2.2.2 Low Voltage Controller

The controller chip is a FPGA from Quick Logic. It will be programmed in anti-fuse technologies. The type name is QL 3012 2 PF 144C. The chip has to be radiation hard. The current design is described with a schematic entry. For the second prototype the design will be modified.

Overview

- Control Bus
  - Port A (input)
  - Port C (input)
    *
  - Port F (output)
- Status input from the Low Voltage Regulators
  - Status plus 7.2 Volt(OC8L)
  - Status plus 3.2 Volt(OC4L)
  - Status minus 1.6 Volt(OC2L)
- Control output to the Low Voltage Regulators
  - Control output plus 7.2 Volt

- Control output plus 3.2 Volt
- Control output minus 1.6 Volt

Interface from the ELMB(Control Bus)

The controller can be accessed from ELMB1 and ELMB2. The access is via the control bus. The control bus consists of an address, a data write, a data read and a control bus.
5 bit data write bus (Port A 0-4) Bit 0 to Bit 4 - Data Bus for the four registers

3 bit address bus (Port A 5-7)
Bit 5 to Bit 7 - Address Bus for the selection of the Registers.
The selection is for read and write access.

5 bit control bus (Port C 0-4)
Bit 0 to Bit 4 - Control Bus

Bit 0 - CLEAR , resets only the addressed register.
Bit 1 - CLOCK , clock for the selected register. the value of the Data Bus is only registered after a signal change from low to high.
Bit 2 - SET , Sets all five bits of the selected register
Bit 3 - PCLR , resets all four registers
Bit 4 -

5 bit data read bus (port F 0-4)
Bit 0 to Bit 4 , read back Bus. With this Bus one reads back the value of the selected register.

3 bit error message Bus (port F 5-7)

Serial Interface (QSIF)

Protocol of the serial data transfer from USA 15(Crate) to the Power Box.

One Package:

| r/w | aaaa | x1 | ddddd | x2 | ccccc |

r/w = if ’1’ read, else write
a = address (4 Bit)
x1 = extra bit
d = data (5 Bit)
x2 = extra bit
c = crc (5 bit)

Signal lines of the serial interface

sdat in	= input stream
sdat out	= output stream
sdat clk	= data clock
sdat start	= transmission reset
sdat status	= status info
reset	= interface reset

4 signal lines.

Registers of the Controller Chip:

control1	control of the Low Voltage Regulators
err_p8_1	status register of the p8 Low Voltage Regulators
err_p3_1	status register of the p3 Low Voltage Regulators
err_m2_1	status register of the m2 Low Voltage Regulators
control2	control of the Low Voltage Regulators
err_p8_2	status register of the p8 Low Voltage Regulators
err_p3_2	status register of the p3 Low Voltage Regulators
err_m2_2	status register of the m2 Low Voltage Regulators

Control of the interface access

Each of the three interfaces can get the access to the controller when it sends the following sequence to the interface control register(ICR). Each interface has its own ICR. It isn't possible that more than one interface has access to the controller.

step	interface control register(ICR)
1	'000'
2	'001'
3	'000'
4	'010'
5	'000'

The Control of the interfaces is designed and tested.

Decision of the Interfaces

The main interface is the interface to the ELMB. The second interface is the interface to the serial bus.

Function of the Status input from the Low Voltage Regulators

OC8L,OC4L,OC2L , if there is an error on one of the 15 input signals the output of the channel is switched off and does not recover since the status register is reset or the whole chip is reset.

2.2.3 Usage of the ELMB

The ELMB will be used for the control and measurement of the Low Voltage Regulators. Each ELMB has 64 analog input channels and 3 digital ports. The digital ports are the port A with 8 bidirectional lines, port C with 5 outputs and port F with 8 inputs. The ELMB has a CAN bus interface with 125 kbaud transmission rate. We will use 9 ELMB's per one CAN bus.

2.2.4 Low Voltage Regulators

The Low Voltage Regulators have a current regulation that will be adjusted to protect the cables in the feed through. For the voltage and current measurement it is important to know that the ELMB has a maximum measurement input voltage of 5 V. For this reason the voltage before and after the current measurement resistor of the 7.2 V supply will be divided by two. For the 3.2 and the minus 1.6 supply the voltage has not to be divided. The input range will be configurated for voltages from +5.0V to -5.0V.

Chapter 3

Procurement of the Power Boards

3.1 Specification for the Power Boards

After the standard selection procedure a contract was passed to the company Wiener for development and delivery of three prototypes according to specifications given below. In this PRR we request the agreement to go ahead with the production of the final series of 15 boards. Results achieved with the mentioned Prototypes which were delivered in November are given in the subsequent chapters.

3.1.1 Introduction

The power board is part of the HEC-LV Power Box. The Box will be used in the HEC detector of the ATLAS experiment at CERN(Geneva). There are special requirements for the power board, because of the radiation and magnetic environment. A schematic overview is shown in figure 3.1, and a typical circuit diagram is shown in figure 3.2. Explanatory information is contained in the mechanics documentation and drawings.

3.1.2 Environment

Design and components used have to be chosen to operate in the following environment:

Storage temperature : -20^{o}C to +70^{o}C
Operating temperature: 0^{o}C to 70^{o}C

Radiation:
Total ionizing dose: 75 Gray
Neutrons : $1.5 * 10^{12}\ neutrons/cm^2$
SEU : $1.85 * 10^{11}\ hadrons/cm^2$

The radiation limits are valid if the components are from a single lot production. This requirement is part of the contract.

Magnetic Field : 100 Gauss

3.1.3 Features

- To have a safety factor of 100%, two voltage converters for each output voltage should be put in parallel.
- An output monitor signal for each dc/dc-converter shows the correct functioning and in case of an error, that the converter has turned off
- "Power on" soft start; no current spikes at "power on"
- Short and over current protection
- Over temperature shutdown of all DC/DC converters if the temperature is greater than 110^{o}C at the hottest spot.
- Operation in open-loop should be possible
- The switching of the converters should be synchronous
- EMI filtering of DC inputs
- Output filtering for ripple and noise
- Output of DC/DC converters for redundancy are connected with diodes, the regulated voltage is the voltage before the diodes.
- Efficiency better than 80% measured in front of the diodes for the connection of the converters.

3.1.4 Input

The input voltage of the board should be 280V +/- 20 V DC. Each DC/DC converter input line is protected by a separate, replaceable fuse.

3.1.5 Output

Three outputs should be provided:

Output voltage	9V
Output voltage tolerance	+/- 10%
Current range	0 - 25A
Output over current protection *	30A
$U_{max\ error}$ *2	14V

Output voltage	5V
Output voltage tolerance	+/- 10%
Current range	0 - 10A
Output over current protection *	15A
$U_{max\ error}$ *2	14V

Output voltage	-3V
Output voltage tolerance	+/- 10%
Current range	0 - 5A
Output over current protection *	8A
$U_{max\ error}$ *2	-12V

[*] Output will be switched off.

[*2] maximally reachable voltage.

Requirements for all output Voltages over the entire load range:

Line regulation (Vi=Vi,min to Vi,max) :	1%
Load regulation (Io=Io,min to Io,max):	2%
Temperature regulation :	0.05%/^{o}C
Long term drift:	0.02%/1k hours
Output ripple and noise :	lower than 150mV (0 - 30 kHz)
(measured 10 cm after the output ring terminals of the HEC-LV-Power-Board)	lower than 25mV (30 kHz - 30 MHz)

3.1.6 Insulation

Input to case : 1500V DC
Input to output : 1500V DC
Output to case : 200V DC

3.1.7 Geometry

The maximum board size, including cooling plate and connectors, is 220mm *200mm * 50mm. The inflow and outflow of the cooling must be on different sides of the cooling plate.(see Figure 1)

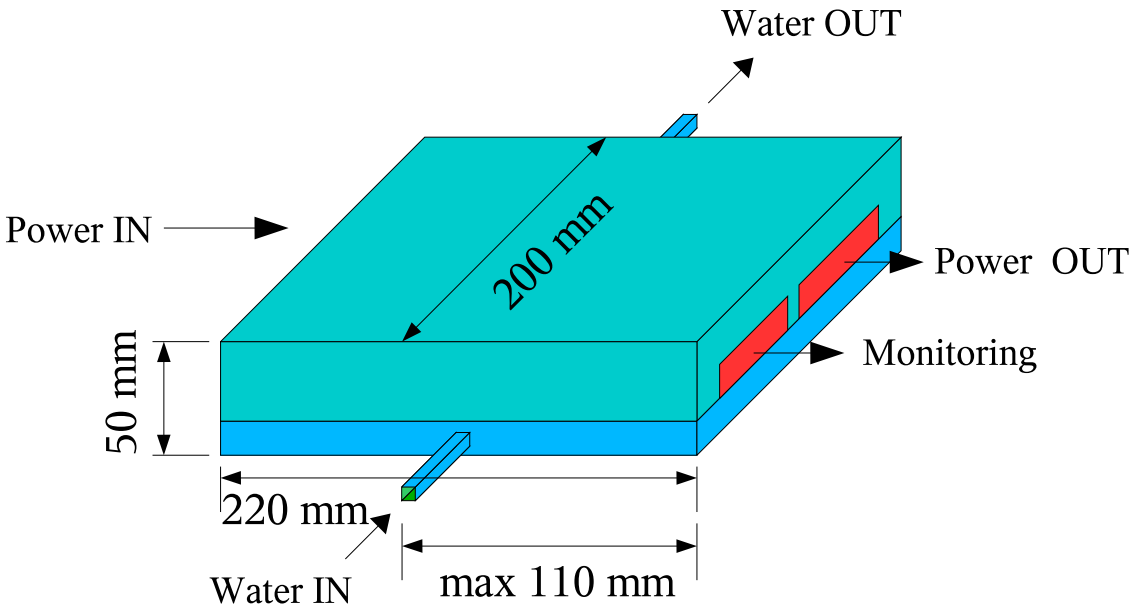


Figure 3.1: Geometrical dimensions and position of connectors

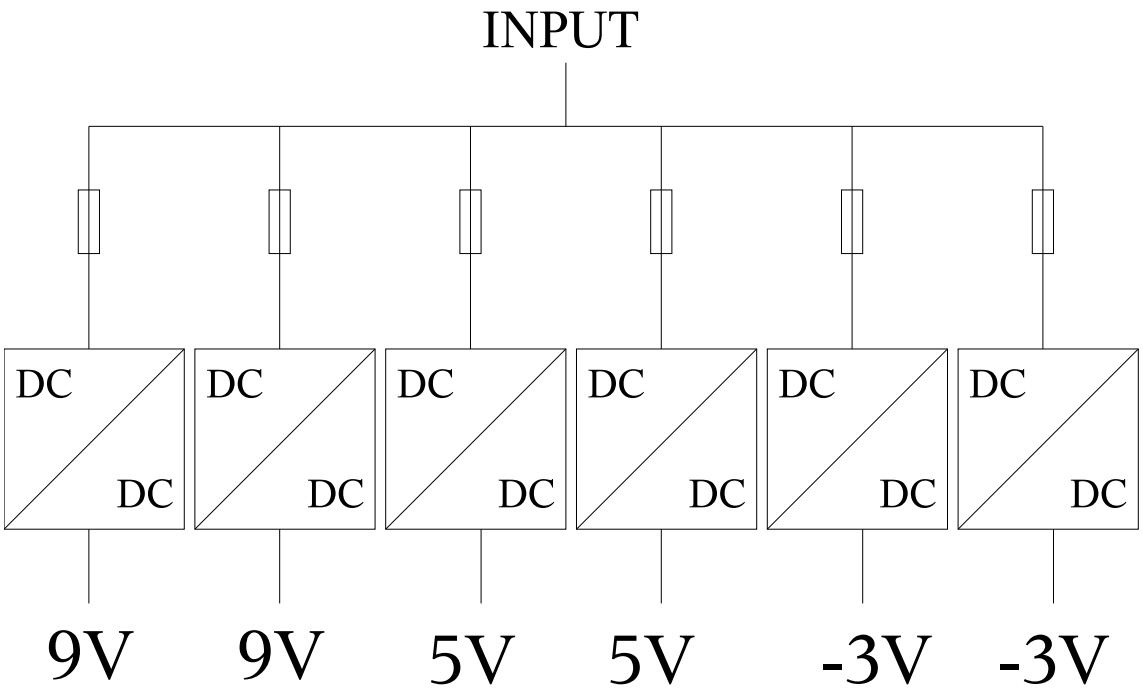


Figure 3.2: Fuses to protect the input line

3.1.8 Interfaces

The Input should be connected with “Federzugklemmen”. On the Output side should be one connector with the monitor signals. For each of the three voltages 4 output cables on 2 output screws will be mounted with ring terminals. There should be one monitor signal for each DC/DC converter, which shows the status. It is an open collector output. If the output is closed, the converter is OK. There should be a temperature measurement resistor at the position of the hottest point. The resistor will be provided by the MPI. The connection have to be for a 4 wire measurement. The monitor connector is a Disconnectable Insulation displacement connector for 1.27(0.05”) pitch ribbon cables. For the required position of the connectors see the figure 1:

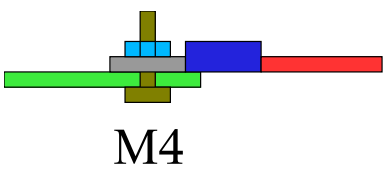


Figure 3.3: Ring terminal

3.1.9 Cooling

The cooling works with a difference pressure of 400 mbar. The smallest diameter in the system is 2.9 mm. The inflow and outflow of the cooling must be on different sides of the cooling plate.(see Fig.1) For in- and outflow of the cooling board a Barbed L fitting from FESTO PNEUMATICS (part no. 12258) should be mounted.

3.1.10 Quality Assurance / Quality Check Procedures

For the first lot a quality assurance plan should be provided. It should describe the tests to be performed by the manufacturer of the prototypes and series modules. All features except the radiation tolerance should be proven on the prototypes by adequate measuring procedures. For the series modules a subset of quality check measurements should be done and documented by the manufacturer.

3.1.11 Documentation

A written Documentation of the HEC-LV-Power-Board has to be provided which describes the functionality, input/output connections and safety. A list of parts, in particular of replaceable objects like fuses, should be added. The QC documentation should be supplied with each board.

Chapter 4

Electronical Test

4.1 Tests done by producer

The producer Wiener tested the 300 V input channels of the power board for EMC connected to a network produced by Rhode and Schwarz, obeying the rules of the EN 55022. The results of the noise test are shown in Fig. 4.1. In this figure L1 is the positive line and N is the ground line. AV stands for average and QP for quasi peak. The solid lines represent the maximum values allowed by the norm.

4.1.1 Output Specifications

On the output channels Wiener measured the ripple and noise to be:

Channel	Current[A]	Ripple and Noise [mV] 0-30 kHz	Ripple and Noise [mV] 30kHz - 30 MHz
9 V	53	3	16
5 V	23	3	22
-3 V	15	1	13

4.2 Tests done at MPI

4.2.1 EMI

In a second set up a HP 11941A Close-Field Probe was used as electromagnetic field sensor. It covers a range from 9 kHz to 30 MHz and is meant to locate sources of electro magnetic interference (EMI).

The different positions of the probe are shown in the following sketch:

The typical noise level is at the level of $0.05\ V/m$. Peaks are visible at multiples of the DC/DC operating frequency. In the frequency spectrum covered the most pronounced noise amplitudes are shown in the following Table. For the final design the presently existing small openings will be closed with a Cu foil. In addition, the power board will be in the fully closed LV power box.

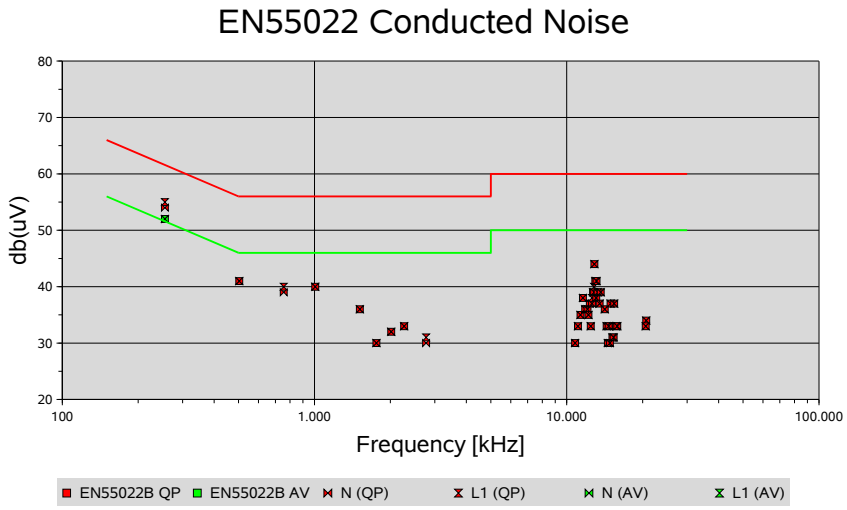
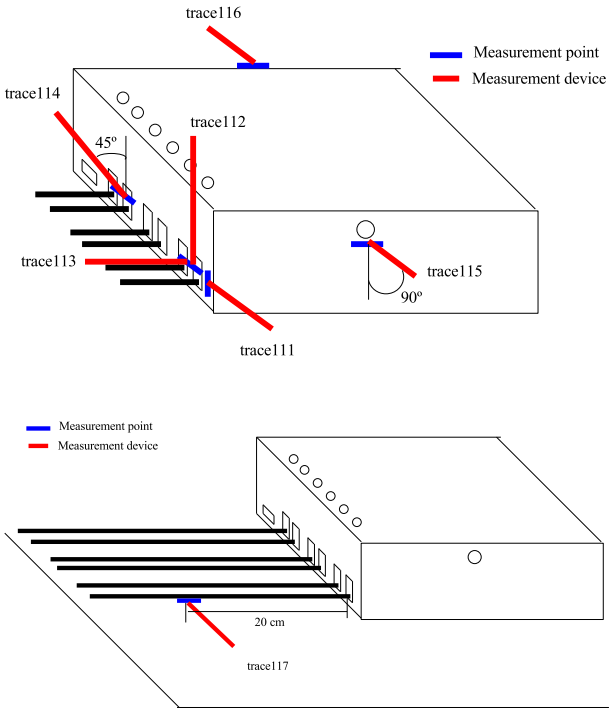


Figure 4.1: Conducted noise as measured by the producer (L1 is the positive line, N is the ground line).

Trace	Frequency [kHz]	Noise Amplitude [V/m]
111	280 20 000	2 0.4
112	280	5.5
113	280 20 000	4.5 0.1
114	280 20 000	1.0 0.04
115	280 560	50 3.5
116	280	40
117	280 560	0.5 0.1
118	280 560 800 1200	4.5 0.5 0.1 0.2



4.2.2 Output Specifications

The output values were measured using adjustable load resistors and were found to be within the specified range (see 3.1.5). Finally we also compared the prototype with the pre-prototype based on VICOR DC/DC converters as used in the combined beamtest in 2004. The noise spectrum has been recorded with the network spectrum analyzer HP 4195A. As an example, the Figure 4.2 shows for the 9 V line the spectrum of the amplitude in dBμV for the frequency range 100 kHz to 100 MHz. The solid line shows the present prototype, the dotted line the comparison with the VICOR pre-prototype: the noise level is typically lower by 20-40 dB, corresponding to a factor of 10-100. Again, the maximum is at the DC/DC converter operating frequency of 280 kHz with about 60 dBμV.

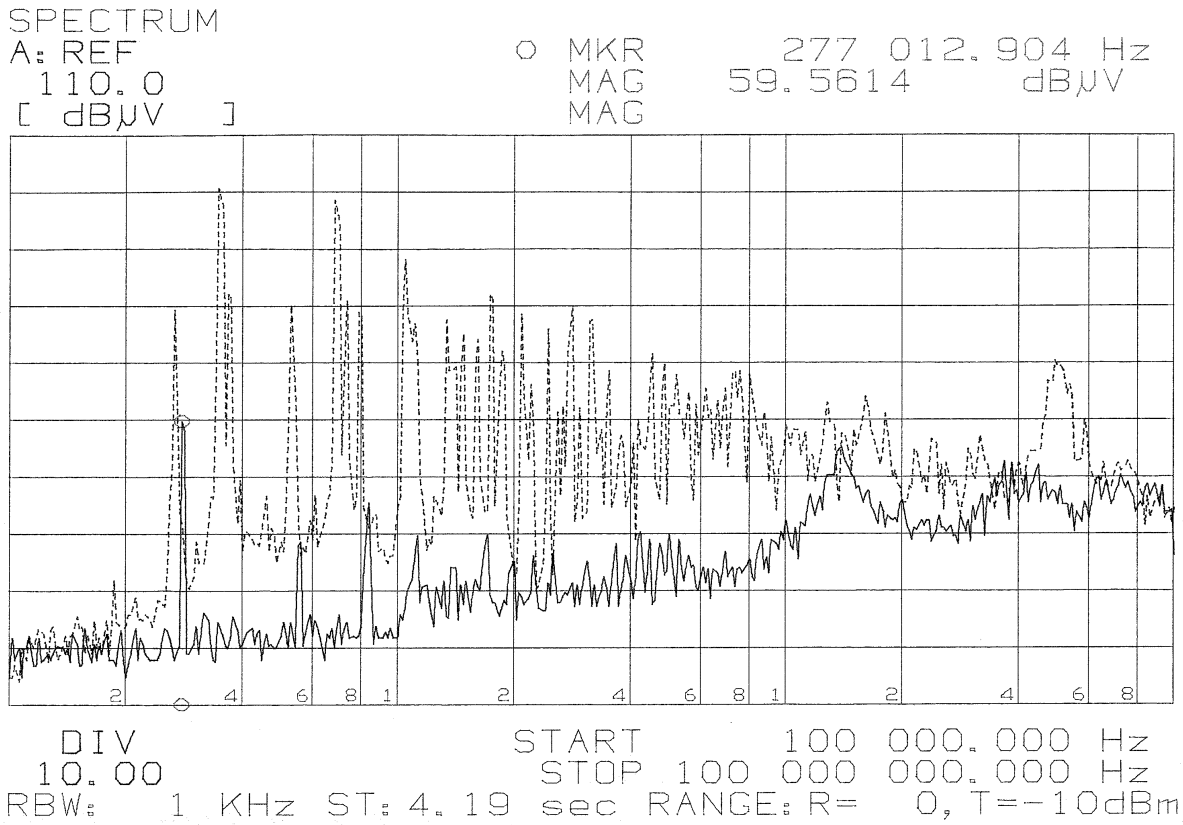


Figure 4.2: Frequency spectrum of the noise amplitude for the 9 V line for the LV PB prototype of Wiener (solid line) and for the preprototype based on VICOR DC/DC converters (dotted line).

Chapter 5

Radiation Hardness

All components of the power box and of the feed-through board have to be radiation hard.
Therefore several tests were done to study the behavior under gamma (Total Ionizing Dose), neutron (Non Ionizing Energie Loss) and proton irradiation (Single Event Effects).

Radiation requirements:
At the position of the LV power box we expect the following level of radiation in 10 years of LHC running and use the following safety factors (SF1, SF2, SF3):

radiation	expected rate	SF1 simulation error	SF2 low dose rate effects	SF3 lot	Total
TID	4.3 Gy	3.5	5	1	75 Gy
NIEL	$3 * 10^{11}\ n/cm^2$	5	1	1	$1.5 * 10^{12}\ n/cm^2$
SEE	$3.7 * 10^{10}\ h/cm^2$	5	1	1	$1.85 * 10^{11}\ h/cm^2$

The safety factor for the lot has been set to 1 because the production is based on the material originating from the same lot as used for the radiation tests.

1. Quick Logic Chip QL3012

- Preselection NIEL and TID: IBR2 (JINR) in 2000)
- Qualification NIEL and TID: IBR2 (JINR) in 2002
- Qualification SEE: UCL in 2002

2. Power board

- Dubna 2004(preselection)
- Dubna 2004(qualification)(NIEL and TID)
- ucl 2005(qualification)(protons for SEE)

Minimum Requirement was reached for all boards and components:

3. ELMB:
See radiation test of ELMB done by CERN.

4. Low Voltage Regulators:
See radiation test done by CERN.

5.1 Quick Logic SEE Test

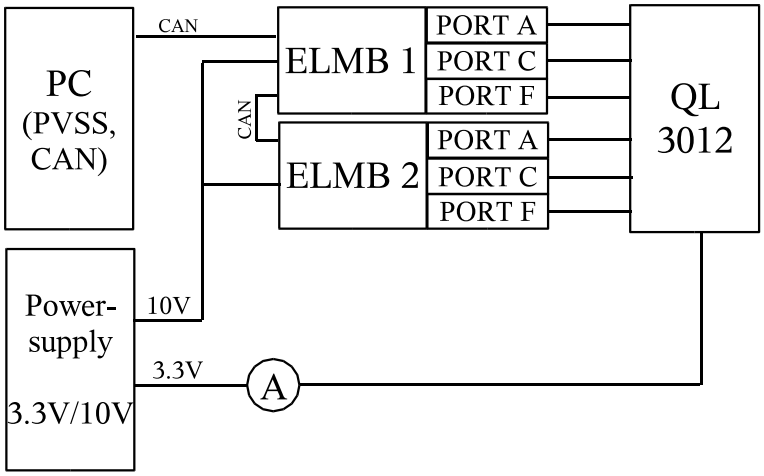
During this Test four Qicklogic FPGAs should be irradiated with Protons, the Energy should be 59 MeV. The name of the FPGA used is QL3012-2PF144C. The reason for this test is to show how are the SEE (Single Event Effect), SEU (Single Event Upset) and Latch-Up Effects. The radiation test was on 26 Feb 2002. Horst Brettel and Joerg Habring has done this test at UCL.

the flux was $2 * 10^8$ ($cm^{-2} * s^{-1}$).

the total applied fluence was $1.8 * 10^{11}$ (cm^{-2})

5.1.1 Test Setup

The test will be done with a PC, two ELMBs plus the Motherboards and the one Board with 4 Chips that should be tested.



5.1.2 Test Procedure

In this test each Chip will be irradiated for 15 minutes, at the start of the test there will a value be written in to one register of the Quicklogic chip. During the test the PVSS software is looking if the value of the register changes. After the 15 minutes the Cables will be unplugged from the QL-chip and plugged to the next QL-chip.

5.1.3 Test Result

In the Test the number of errors and the current of the power supply was logged.
You see, that the number of errors is not very big.

Chip	Errors
1	1
2	0
3	1
4	0

During the 15 minutes the current hasn't increased.

Chip	Current[mA]
1	2.5
2	2.5
3	2.5
4	2.5

Chip number 4 was irradiated 28 minutes. It has the same behaviour as the other 3 chips. But after 19 minutes the current started to increase. The maximum was 170 mA, 7 minutes after switch off the current was at 16 mA.

Time[min]	Current[mA]
0	2.5
15	2.5
19	3.3
28	170
beam has been switched off	
35	16

5.2 Quick Logic TID and NIEL Test

At JINR/Dubna 10 QL chips have been irradiated and proven to operate without deterioration (worst case) up to:

- TID 130 Gy
- NIEL $6 * 10^{12}\ n/cm^2$

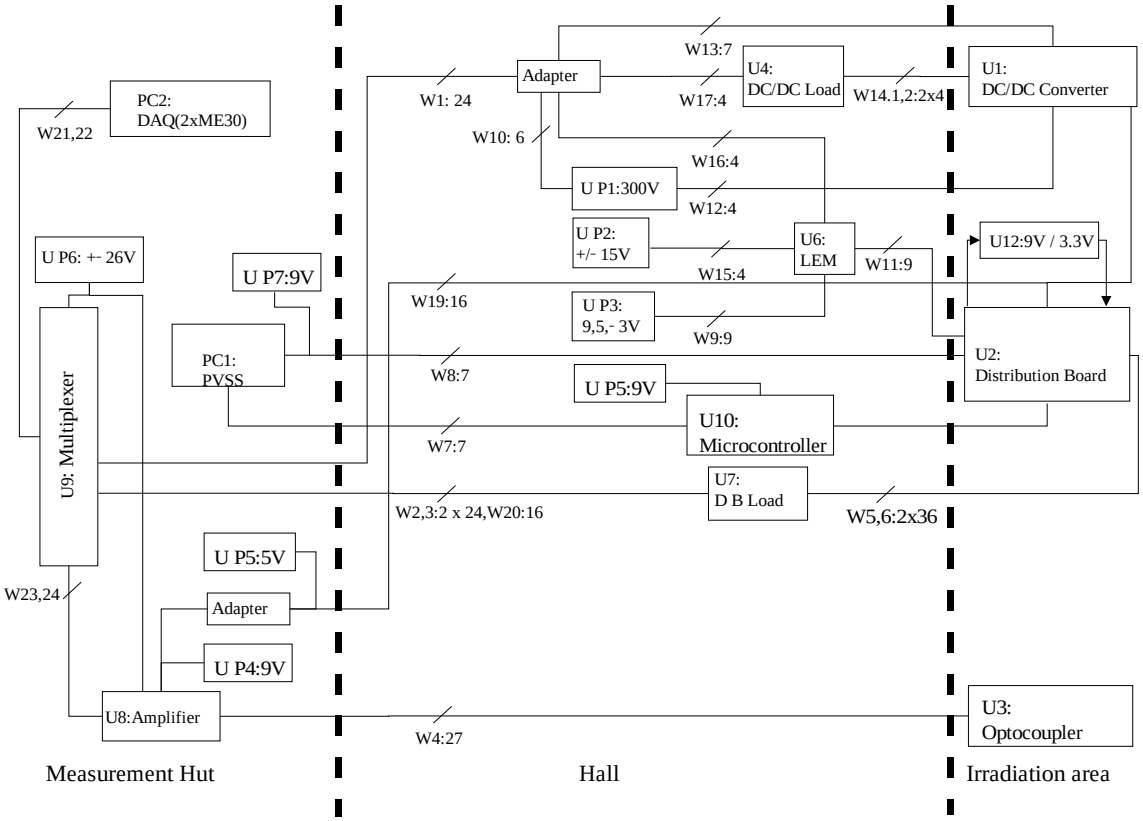
For details of this test see:
HEC Note167
Thus we expect for the QL chips an additional safety factor of at least 1.7 and 4 for TID and NIEL respectively and an error rate due to SEE of 0.5 failure for 10 years LHC operation.

5.3 Power board NIEL and TID Test

At the pulsed neutron source IBR-2 at JINR/Dubna the power board was irradiated with Neutrons and Gammas.
This was done for the first time in September 2004 with a prototype existing at Wiener, it was made for an other purpose, but basically fulfilled the same specifications.
We tested some of its components separately, giving us the possibility to change them if needed. Specially the power MOSFETS had never been used in an environment with such radiation. The 900 V version of the MOSFET which was already used in the module proved to be more radiation hard than a 450 V version which was also tested.
The breakdown of the board was not caused by a failure of the power MOSFETS (they survived a higher dose) but probably due to radiation damage on the control transistors.
Thus it turned out not to be necessary to change anything, since the foreseen version fulfilled the specifications concerning radiation hardness.
In a second test in December we irradiated a board which already was built as specified by us, using components of the final lot.

5.3.1 Test Setup

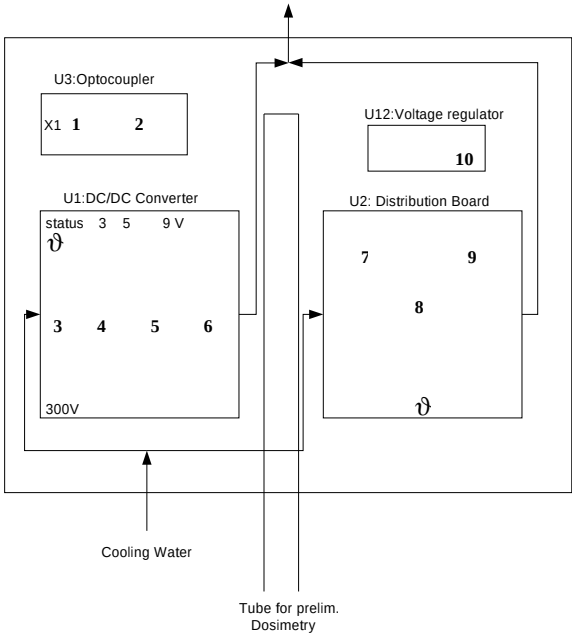
Overview



We measured the output voltages of the board over resistors, which were chosen to yield the later upcoming currents (16/8/4 A).
The 9V channel was connected to 0.56Ω, the 5V to 0.68Ω and the -3 to 0.5Ω
To measure the DC/DC Converter input current a current converter was used, it was a LEM current transducer HY 5-P.

5.3.2 Dosimetry

Irradiated Module

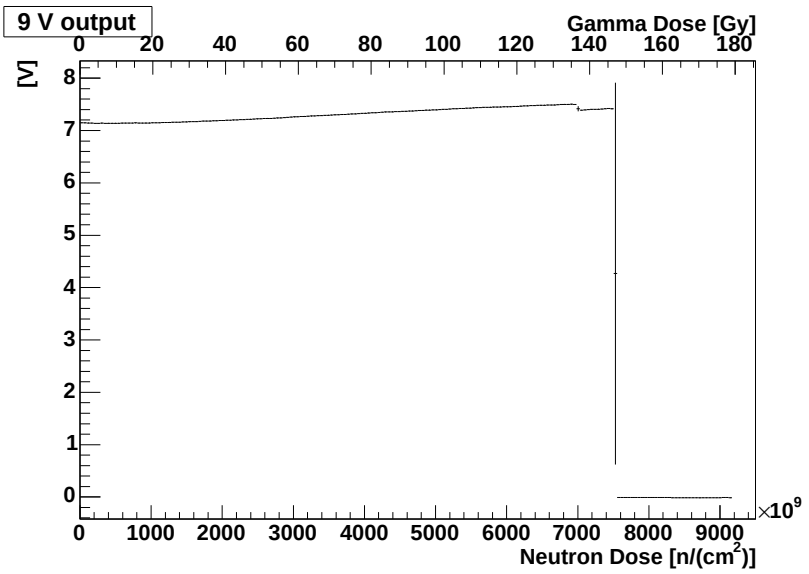


The three Modules were put in a box of 0,5 mm Cd foil for n/γ conversion and the mounted on a Al plate. This was done in order to achieve a n/γ ratio which is closer to the one predicted in the ATLAS radiation simulations.
Eventually this modification complicated the dosimetry and therefore we only have first preliminary data. We expect the final values for the fluxes to be significantly higher.
The preliminary fluxes are:

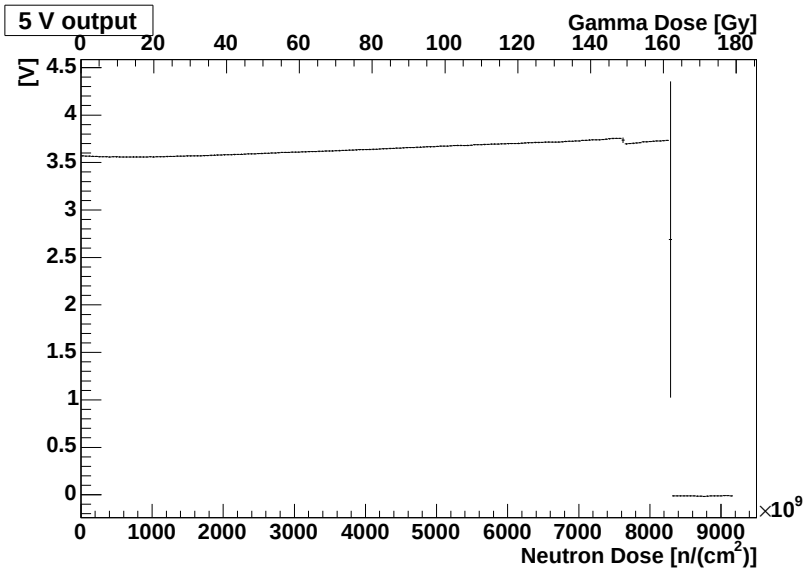
- γ : $5.40\ Gy/h$
- n: $7.6 * 10^{12}\ n/cm^2 s$

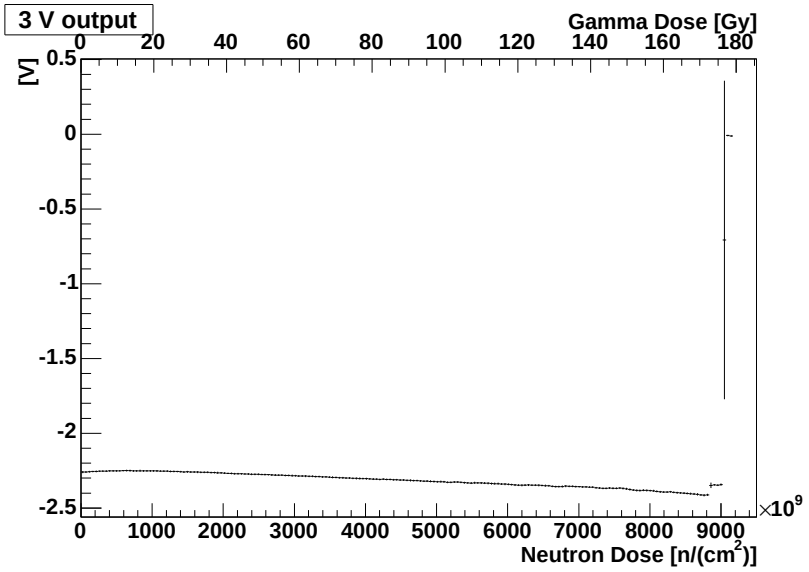
5.3.3 Results

The different output channels of the power board broke down between $7.3 * 10^{12}$ n/cm^2 and $9.3 * 10^{12}$ n/cm^2, and 143 Gy and 184 Gy respectively.
In the former radiation test the prototype of this power board survived a integrated dose of neutrons and gammas, which was about a factor two higher. We expect the same results in this test once we get the exact analysis of the dosimetry team.
Plotting the histograms one can see the behavior of each channel. The errors shown are the spread errors of the single bins.



The output voltage on the yaxis is reduced due to the long cables coming from the reactor to the counting hut. The data is not corrected for that, since this setup was not meant to measure the output precession, but only the behavior under radiation.
Short before the total breakdown one can spot a slight drop in the output voltage, which is due to the breakdown of the first DC/DC converter in the channel. The second converter suddenly is confronted with a bigger load.


5 V output
Gamma Dose [Gy]
0 20 40 60 80 100 120 140 160 180
[V]
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
×10^9
0 1000 2000 3000 4000 5000 6000 7000 8000 9000
Neutron Dose [n/(cm^2)]


3 V output
Gamma Dose [Gy]
0 20 40 60 80 100 120 140 160 180
[V]
0.5
0
-0.5
-1
-1.5
-2
-2.5
×10^9
0 1000 2000 3000 4000 5000 6000 7000 8000 9000
Neutron Dose [n/(cm^2)]