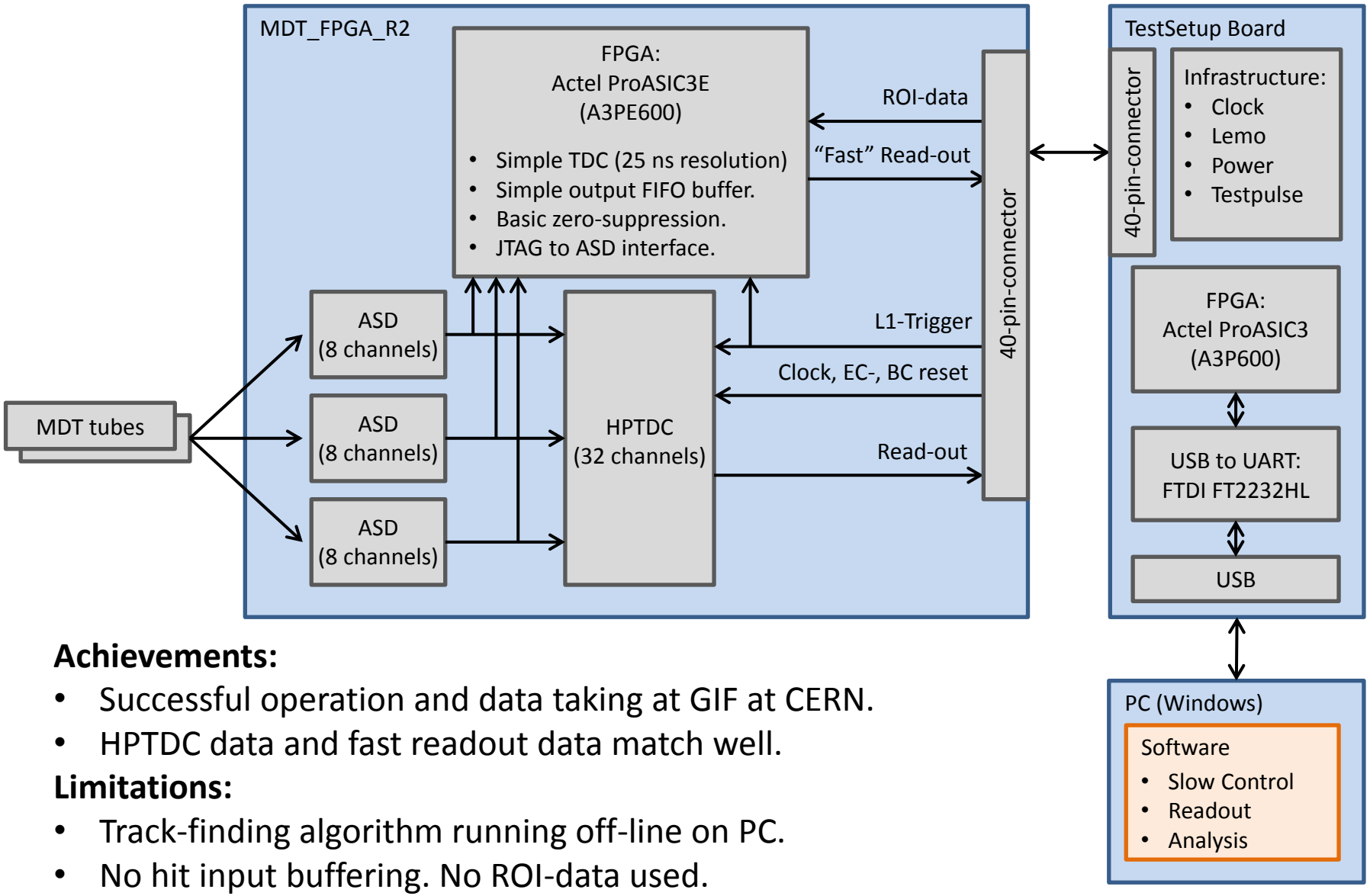
The MDT Trigger Project - Outline

- New Mezzanine Card for Generation of Trigger Data Using an FPGA
- Readout Hardware: TestSetup Board
- Next Setup: Based on GLIB V3 from CERN
- Explanation of TDC Mechanism
- Limitation and Possible Improvements

New Mezzanine Card for Trigger Data Generation



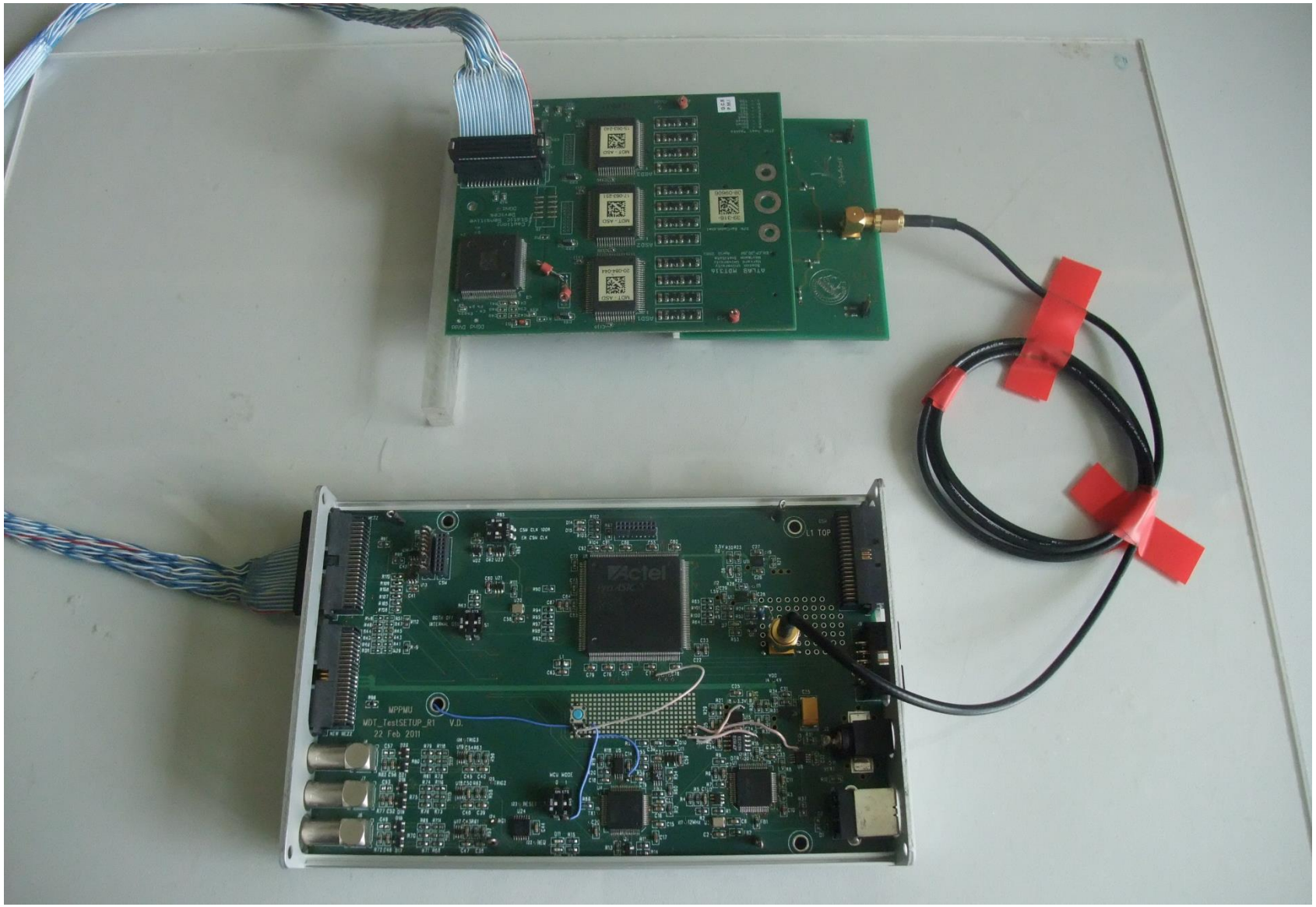
Achievements:

- Successful operation and data taking at GIF at CERN.
- HPTDC data and fast readout data match well.

Limitations:

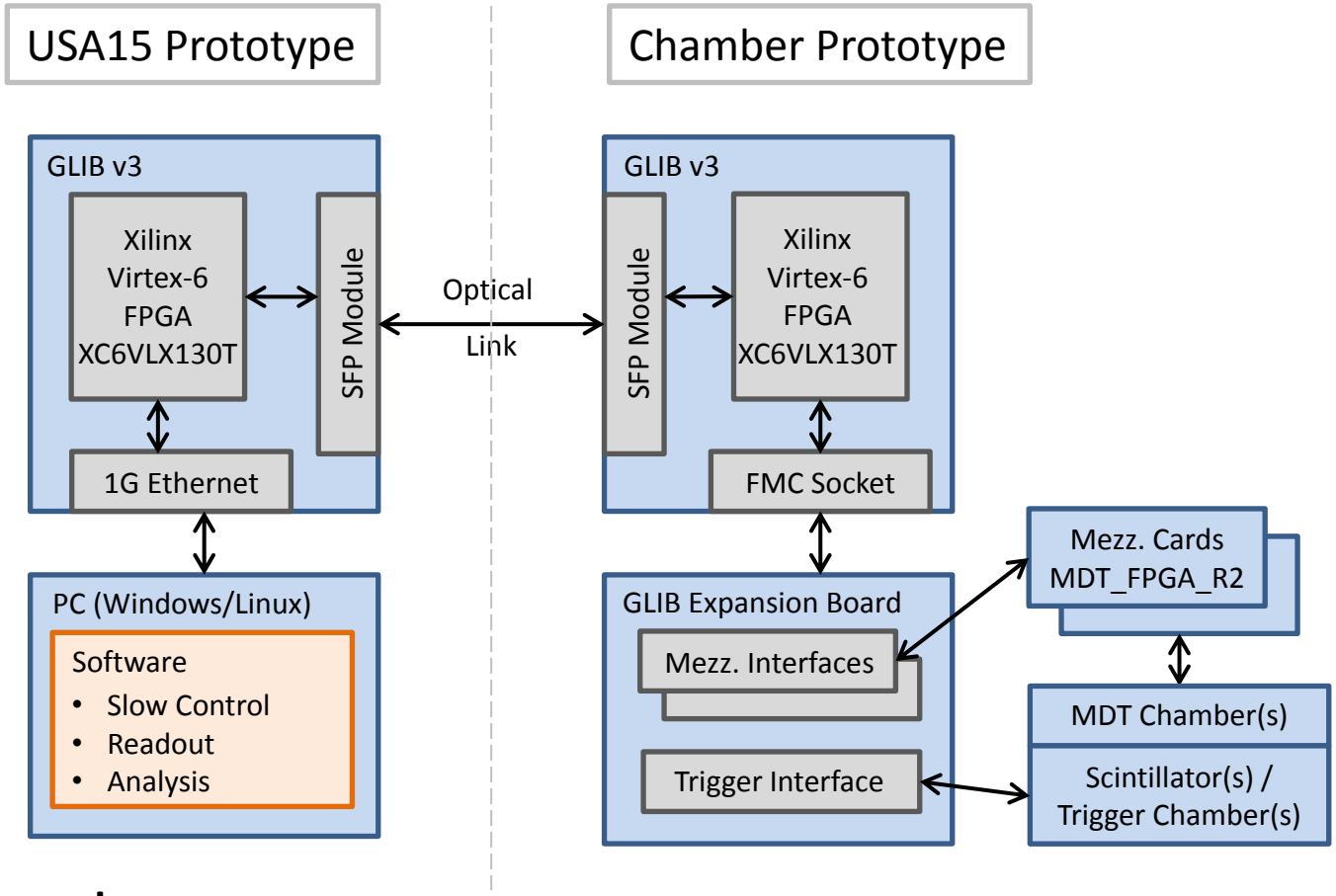
- Track-finding algorithm running off-line on PC.
- No hit input buffering. No ROI-data used.
- Limited bandwidth due to USB.

TestSetup Board (TSB) with “Old” Mezzanine Card



The TSB is used to characterize the AMT/HPTDC and to read out the first trigger data.

MDT Trigger Prototype Scheme Using the GLIB v3



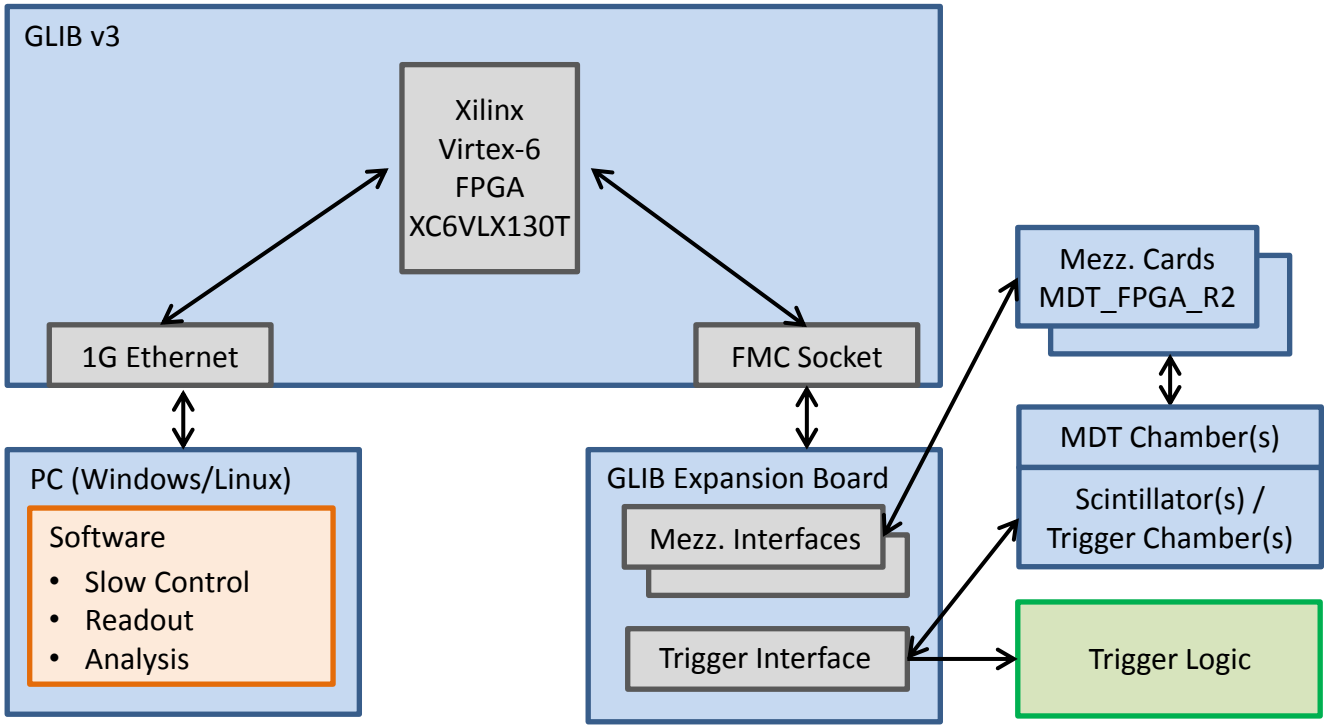
Use cases of the setup:

- Prototype of new CSM with GBT optical interface for read-out + slow control.
- Light-weight test system for old and mezzanine cards.
- Demonstrator for MDT trigger with 2 mezzanine cards.

Status:

- Concept-level. 2 GLIB v3 boards available, 8 additional have been ordered.

MDT Trigger Prototype Simplified Scheme Using the GLIB v3



Use cases of the setup:

- Light-weight test system for two mezzanine cards (maybe more in future version).
- Prototype for track-finding and trigger algorithm in hardware.

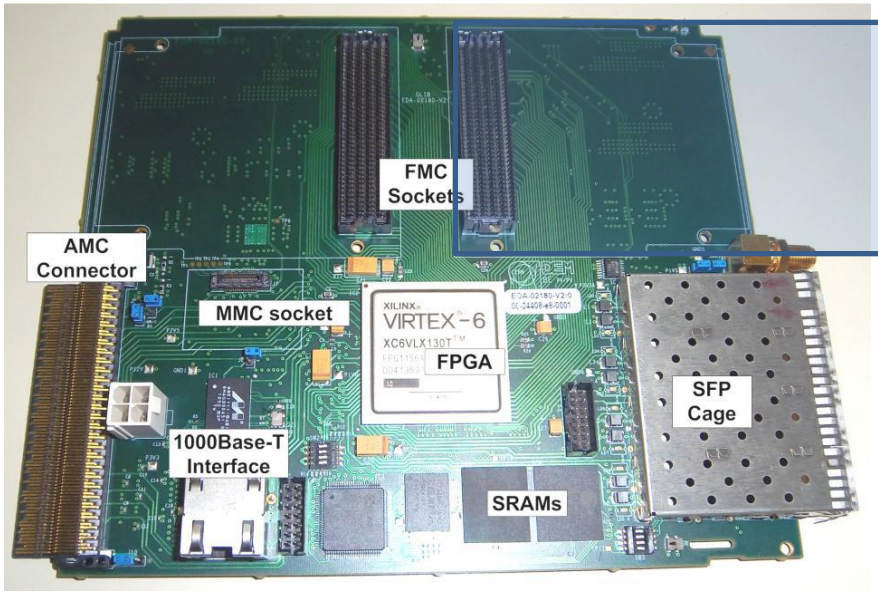
Status:

- Schematic of expansion board ready, layout starting.
- Firmware development started, first basic features implemented, FPGA ~25% full.
- Concept for new software ready. Coding ongoing with HW/FW development.

GLIB FMC Expansion Board for Trigger Demonstrator

"New" mezzanine card (MDT_FPGA_R2) with HPTDC and FPGA. It can generate trigger data.

"Old" mezzanine card (MDT316) with AMT and no FPGA.



GLIB FMC Expansion Board

- Power Supply
- LHC clock, L1 trigger
- Scintillator(s) / Trigger Chamber(s)
- Trigger Logic

- Connect mezzanine cards with or without trigger feature.
- Control and read out via GB Ethernet.
- Demonstrator for new CSM incl. trigger.
- Demonstrator for GBT link.

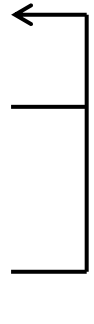
Trigger Data Generation on the Mezzanine Card – Simple TDC

Simple TDC implementation:

- Verilog code, ~ 1300 lines of code (total FPGA: ~ 3100 lines).
- It measures the time in 25 ns steps (40 MHz clock) between the rising/falling edge of a MDT hit and the L1 trigger (or any other) signal.
- 24 channels, all working in parallel, i.e. indenedently of each other.
- Rising and falling edges are handled independently.
- Simple zero-suppression implemented: Counter values of 0 can be ignored.

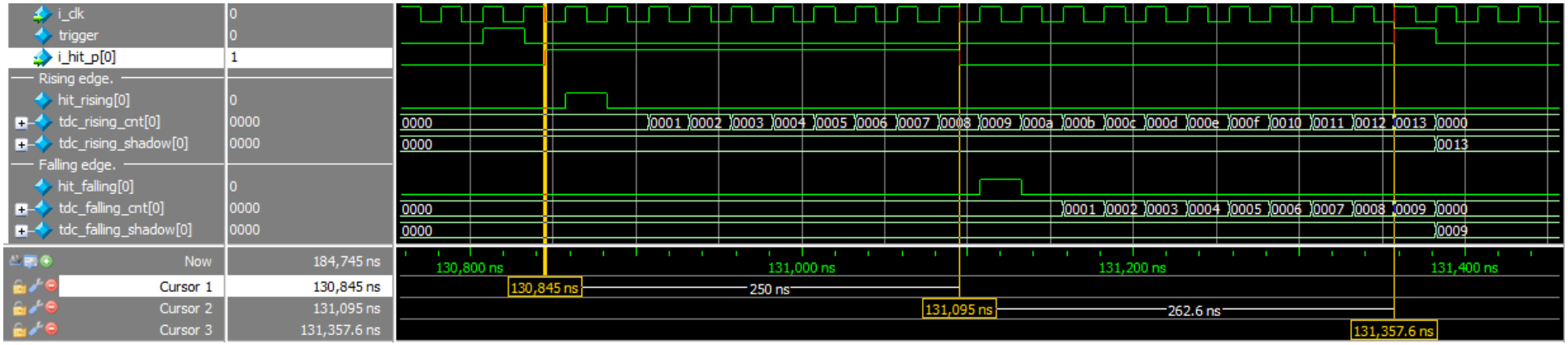
Simple TDC working scheme:

- When a rising/falling edge of a hit signal is detected, a counter is started.
- On a L1 trigger, the counter value is copied to a shadow register.
- The counter is re-armed to react on the next rising/falling hit signal.
- The value is sent to the readout-buffer.
- If there is no L1 trigger within a programmable the time-out limit, the counter value is discarded and the counter is re-armed.



Example simulation shown on next slide.

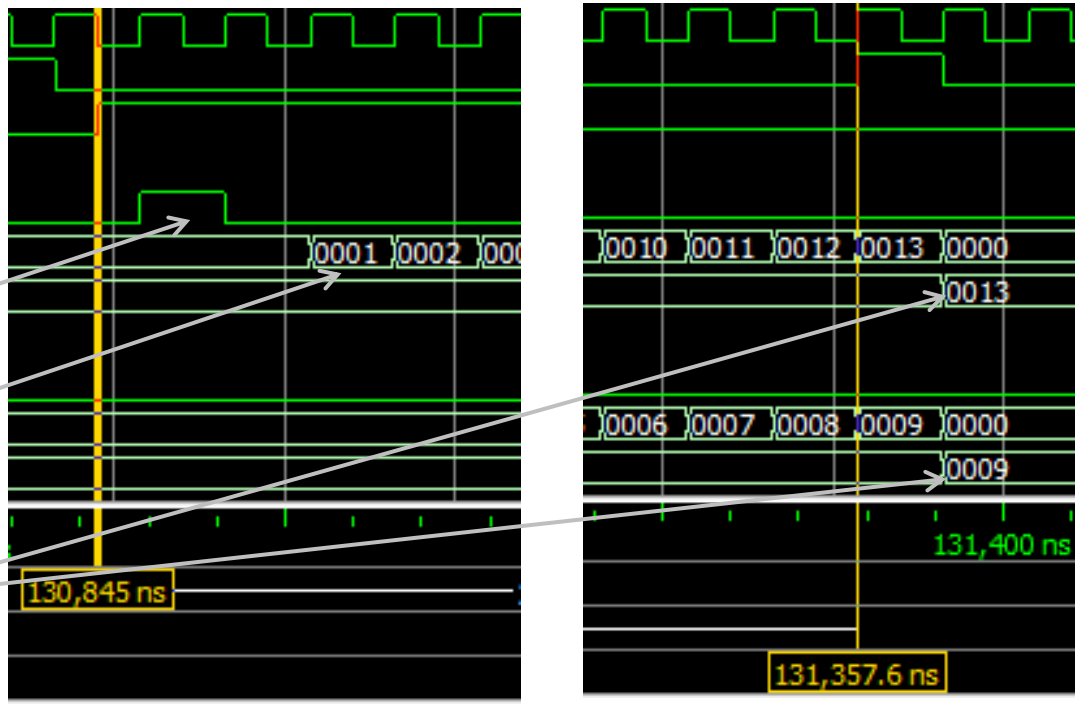
Trigger Data Generation on the Mezzanine Card – Simple TDC Simulation



- 40 MHz Clock.
- Positive hit pulse, 250 ns wide.
- Trigger 500 ns after pulse.

⇒ Pos edge: 0x13 = 475 ns.

⇒ Neg. edge: 0x9 = 225 ns.



Simple TDC – Improvements and Alternatives

Limitations:

- There are no TDC buffers.
  => After a hit, the channel is “blind” until it is re-armed. Thus, hits can get lost.
- No region-of-interest (ROI) information is used for data reduction.
- For the first test, the setup was completely stopped after a L1 trigger until all values had been read.
- => Limited trigger rate.

Possible Improvement:

- Implement buffering scheme in order to cope with a given number of hits within a certain time window.
  => Much more complicated, danger of bugs.
- Use ROI-information for further data reduction.
  => Interface to trigger chambers necessary + more complex.

Possible Alternatives:

- A new TDC chip with a second, independent “fast” data channel with lower time resolution.
  => TDC development required, big effort!
- Store hit data in a memory for a certain time. On request, copy a given part of the memory to an output buffer and transmit the data.
- Continuous streaming of hit-data in real-time.
  => Simple solution + no hits will be lost.

Conclusions

- First tests done with “new” mezzanine card and TestSetup Board. But too “small” for further steps.
- New hardware: GLIB v3 + expansion board
- Next big step: Implementation of track finding and trigger algorithm on FPGA
- Evaluate improvements/alternatives for fast TDC on mezzanine cards