

## The new octal amplifier-shaper-discriminator chip for the ATLAS MDT chambers at HL-LHC

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### Abstract

In order to fully exploit the physics potential of the ATLAS experiment at the HL-LHC, the trigger rate of and maximum latency of the first-level trigger system will be increased to 1 MHz and 10  $\mu$ s, respectively. In addition, a new first-level muon track trigger with high momentum resolution based on the ATLAS precision Muon Drift-Tube (MDT) chambers will be employed which requires triggerless readout. The TDC ASICs of the current front-end electronics of the MDT chambers are incompatible with these requirements. The front-end boards, each with a TDC chip and three 8-channel amplifier-shaper-discriminator (ASD) chips have to be replaced. Therefore, a new octal ASD2 ASIC has been developed in modern 130 nm IBM/Global Foundries CMOS technology. The chip also contains a Wilkinson ADC to perform both time-over-threshold and signal charge measurement. The ASD design has been fully qualified for the serial production of 80000 chips for ATLAS. The performance in terms of signal rise time and channel uniformity significantly surpasses the one of the previous chip while keeping the power consumption constant. In addition to the characterisation with test pulses, several chips have been mounted on the front-end boards and tested in a muon beam at the Gamma Irradiation Facility GIF++ at CERN up to high counting rates where the superior drift time and spatial resolution becomes evident.

**Keywords:** MDT chambers, ASD chip, High-Luminosity LHC, ATLAS experiment

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### 1. Functionality

The first processing stage of an ATLAS Monitored Drift Tube (MDT) readout electronics, the Amplifier-Shaper-Discriminator (ASD), largely determines the overall performance of the MDT chambers for crucial parameters like time resolution, channel uniformity, efficiency and noise rejection. The MDT ASD is an 8-channel amplifier-shaper-discriminator ASIC with charge-to-time converter based on a Wilkinson ADC which has a variety of programmable parameters: the discriminator threshold and hysteresis, the channel dead-time, the charge integration time and the capacitor discharge current of the Wilkinson ADC. The ASD2 prototype design is done in the well-established and supported, radiation tolerant 130nm IBM CMOS 8RF-DM technology on the basis of the original ASD design features [1].

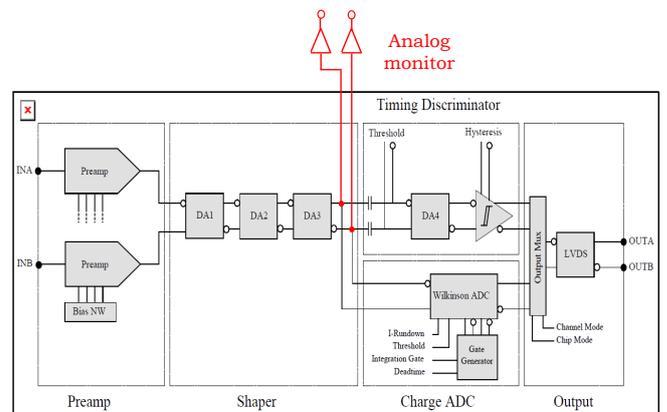


Figure 1: Functionality of the existing ASD and the future ASD2 chip for the ATLAS MDT chambers at LHC and HL-LHC, respectively.

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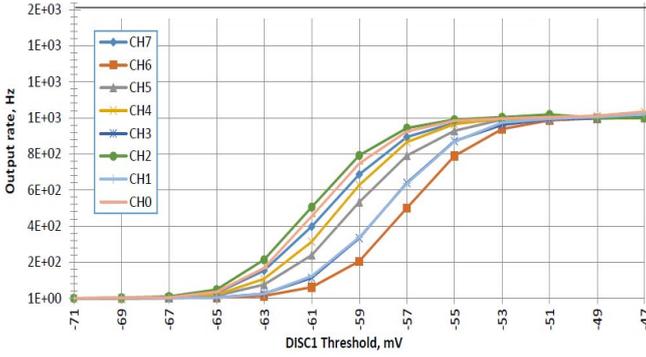


Figure 2: Discriminator threshold scans of the 8 channels of a typical final ASD2 chip.

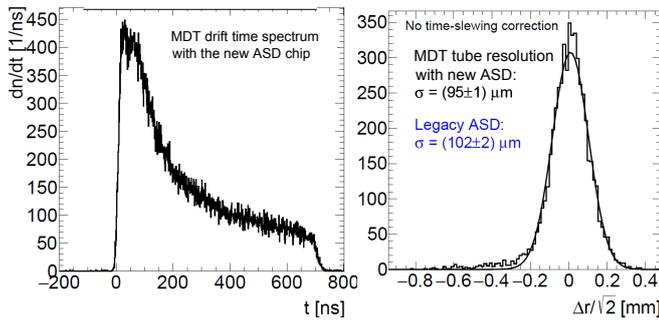


Figure 3: Drift time spectrum (left) and spatial resolution (bottom) of MDT drift tubes in a muon beam at CERN read out with the final version of the ASD2 chip.

The ASD provides two modes of operation: Time-Over-Threshold (ToT) and ADC mode. Each ASD channel comprises an input stage, a charge sensitive preamplifier converting the input charge into a voltage, followed by three shaping stages, discriminator and the Wilkinson-type ADC, which is enabled depending on the operation mode. In ToT mode, the discriminator output is directly routed to the channel output pins. It reflects the crossing of the programmed threshold by the amplified and shaped signal. In the experiment, this threshold crossing determines the arrival time of the ionization charges at the sense wire of the drift tubes. But because of finite rise time and bandwidth, the threshold crossing time depends on the signal charge and on the threshold itself. The ADC charge measurement is used to reduce this dependence in order to increase the accuracy of the time measurement (time slewing corrections).

The ADC measures the signal charge in a given time window following the initial threshold crossing (charge integration gate) using the dual-slope Wilkinson technique where the amplified input charge is collected on a capacitor during the programmable integration window and then converted into a digital pulse width corresponding to the discharge time of the capacitor at a programmable discharge current (rundown current). Each ASD channel provides a differential digital output, where the time of the leading edge corresponds to the ionization charge arrival time and the pulse width represents the charge in the leading edge of the input signal. This timing information is subsequently digitized by a TDC ASIC.

The ASD design uses a common DAC to provide the threshold for all 8 discriminators on the chip. Great emphasis was put on minimizing channel-to-channel gain variation and internal offsets, to reduce intrinsic channel noise and crosstalk and to achieve high uniformity of the operating parameters among the channels of each chip (see [2] for more details on a previous version of the chip). The analog path was modified and made fully differential compared to the original ASD ASIC, where the preamplifier consisted of a single-ended (i.e. common source) analog gain stage with feedback capacitor. Post-layout simulations validated this choice, demonstrating that unwanted supply noise is attenuated of -7dB at the output of the first stage. The ASD2 ASIC occupies an area of 7.64 mm<sup>2</sup> and has a sensitivity of about 10 mV/fC, 10 ns peaking time at the discriminator input and 10 mA current consumption per channel at 3.3 V supply voltage.

## 2. Performance Tests

A full characterization of 18 chips has been performed. The test results (see for example Fig. 2) show excellent uniformity of the parameters of all channels on a chip (only 3-6 mV maximum threshold spread) and also between different chips (only 8 mV threshold spread), a factor of 3 better than for the original chip made in 500 nm HP CMOS technology [1]. The laboratory test results (on- and off-chamber) agree very well with the post-layout simulations for all performance parameters. Test-beam data taken with a small MDT chamber at CERN with and without  $\gamma$  background irradiation show that the new ASD2 ASIC performs equally well as the original chip on muon and  $\gamma$  signals with respect to drift time and spatial resolution (see Fig. 2). The peaking time is 2 ns shorter than for the original chip resulting in a slightly improved spatial resolution of the drift tubes. An irradiation test of the latest version of the chip at CERN showed no degradation of the functionality and performance for  $\gamma$  irradiation doses up to 1 MRad as expected for the 130 nm CMOS technology used.

After having successfully passed the required tests, the production of the 80,000 ASD2 chips required for the ATLAS MDT electronics upgrade for HL-LHC is foreseen in 2019-2020.

## References

- [1] Y. Arai, et al., ATLAS Muon Drift Tube Electronics, *J. Instr.* 3.09 (2008) P09001.
- [2] M. De Matteis, et al., Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC, *J. Instr.* 11.02 (2016) C02087.