Use of Triple Modular Redundancy (TMR) Technology in FPGAs for the Reduction of Faults due to Radiation

Implementation in the ATLAS Monitored Drift Tube (MDT) Readout FPGA

M. Fras, H. Kroha, O. Reimann, R. Richter, A. Rudert B. Weber
Max-Planck-Institut für Physik, Munich, Germany

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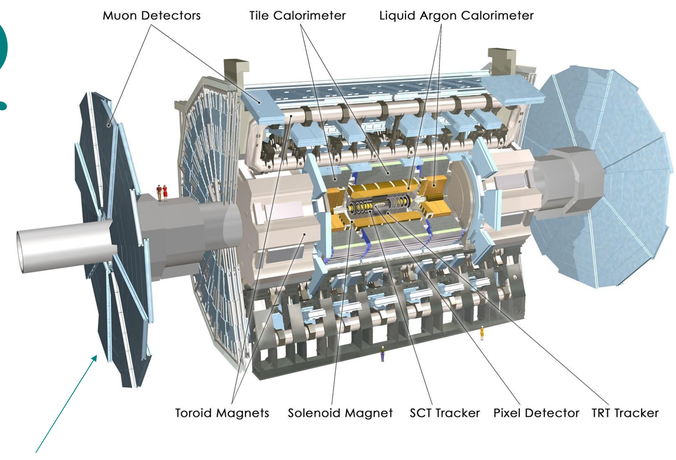
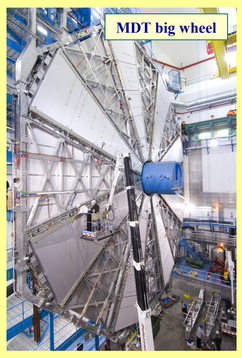
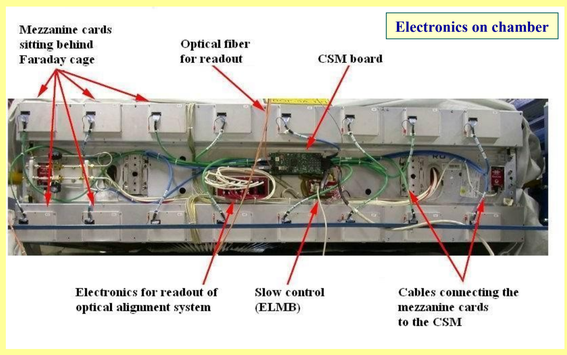
Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)



MDT big wheel

ATLAS Muon Spectrometer: Monitored Drift Tubes (MDT)

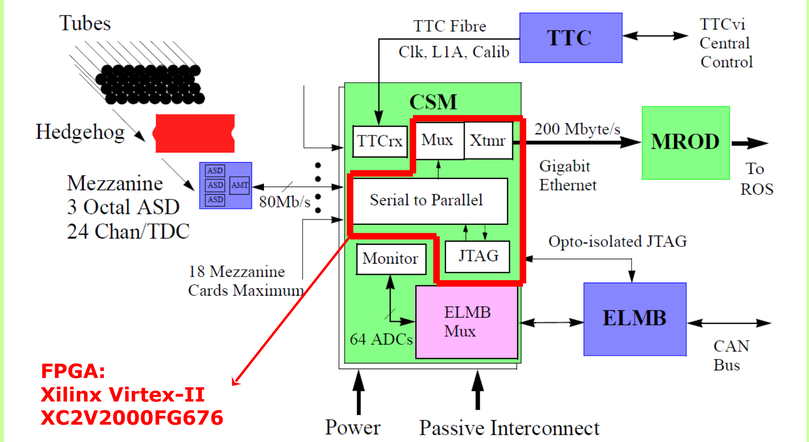




MDT chambers at ATLAS
- 1150 chambers
- 1102 CSMs
- 14218 mezzanine cards
- 353952 tubes

Components of a MDT chamber:
- Up to 432 tubes with 30 mm diameter
- 18 mezzanine cards
- One chamber service module (CSM)
- One slow control interface (ELMB)
- Alignment system
- Gas and high voltage connection

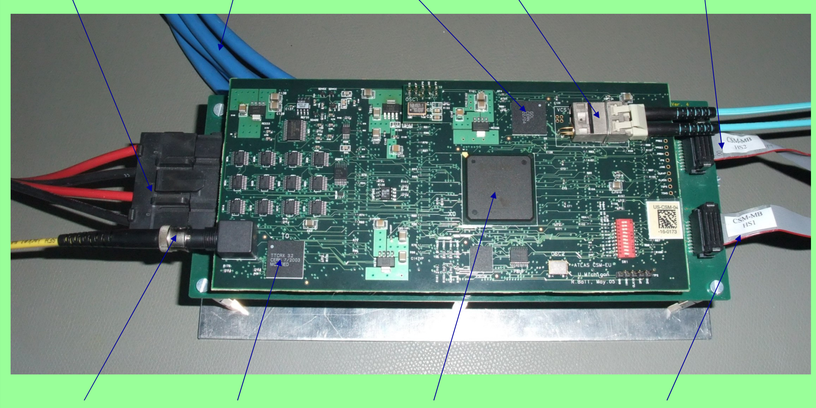
Overview of Monitored Drift Tubes (MDT) System



How the muon system works:
- Muons are detected by ionizing the gas in the tubes leading to a charge pulse
- The signals are digitized by the ASD chip on the mezzanine card
- The drift time of the hit is measured in the AMT chip
- The drift time data are sent to the CSM, which multiplexes them onto an optical link to the readout system (MROD)
- The CSM receives power, slow control, LHC clock and trigger information which it distributes to the 18 mezzanine cards

Control and Readout Link Unit: Chamber Service Module (CSM)

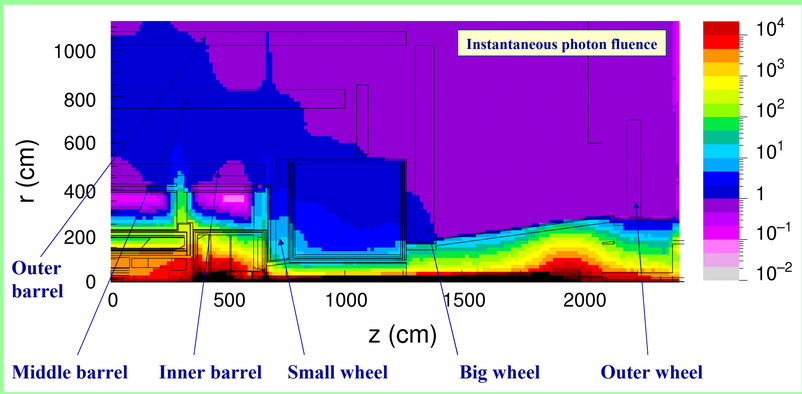
Power connector supplying CSM and mezzanine cards
Cables to mezzanine cards
1.6 GBps Serializer ASIC (GOL)
Optical link to readout system (MROD)
SPI Interface for readout of temperatures



Optical Link providing LHC clock and trigger
LHC-Clock and Trigger Receiver ASIC (TTCRX)
Xilinx FPGA Virtex-II 2000 XC2V2000FG676
JTAG-Interface to slow control (ELMB)

CSM main functions:
- Provide control and monitoring of operation parameters
- Continuously receive serialized data from mezzanine cards
- Process and multiplex data to readout system

Radiation Environment for MDT Front-End Electronics

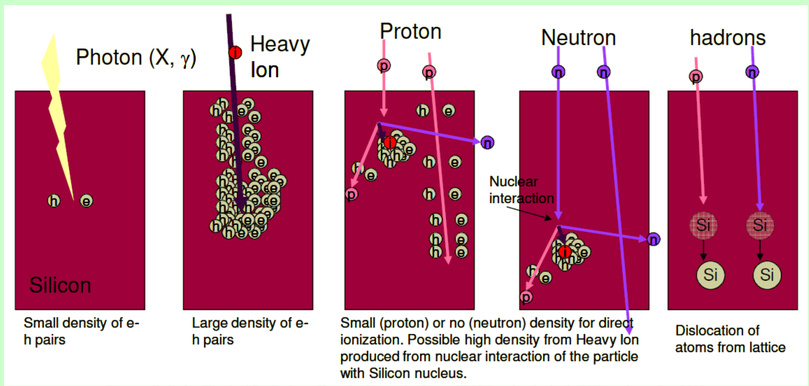


Radiation affecting CSM:
- CSM will be exposed to radiation environment like MDT tubes
- Radiation level strongly depend on location

Simulated radiation environment with safety-factors for 10 years of LHC operation:
- TID: 6.24 kRad = 62.4 Gy
- SEE (Single Event Effect): 2.67 · 1010 n/cm2

Estimates from irradiation test done by R. Ball, T. Dai, J. Chapman in 2005
- TID for CSM FPGA ~ 45 kRad = 450 Gy
- About 90 configuration SEUs lead to CSM operation disruption
- Projected 1.4 disruptions per hour within all 1102 CSMs

Radiation Effects on Electronics



Source: Federico Faccio, "Radiation effects in deep submicron CMOS technologies", ESE seminar, Jan 2010

Special Case: Radiation Effects on SRAM-based FPGAs
- User Data SEU (Single Event Upset)
  E.g. Corruption of data, parity error, invalid state in FSM, possible lock-up of cor
- Configuration SEU
  Changes to the FPGA configuration cells can change device functionality.
- FPGA SEFI (Single Event Functional Interrupt)
  Failure of support circuit, e.g. JTAG TAP, reset or configuration block, clock gen
  Often leads to complete malfunction of device.
- Silicon Effects (Surface + Bulk)
  E.g. Latch-up, degradation of semiconductor elements, increased power consumpti
  partial or total malfunction, physical destruction

Severity
Likeliness

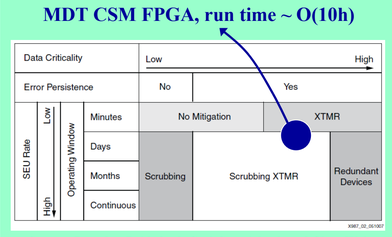
Possible Remedies for Radiation Effects

General mitigation methods for FPGAs
- User Data SEU
  => TMR (Triple Module Redundancy)
  => Failsafe FSMs
  => Use 2 or more redundant devices
- Configuration SEU
  => Configuration Readback
  => Scrubbing (re-write configuration bits)
  => (TMR)
- FPGA SEFI
  => Re-configuration of FPGA
  => Power cycle
  => External watchdog circuit
  => Redundant devices
- Silicon Effects (Surface + Bulk)
  => Shielding
  => Radiation Hard Technology (Virtex QPro, Anti-Fuse, Flash-based, ASIC)
  => No SEL observed in Virtex-II up to 19 kRad accorsing to XAPP989 (v1.0)

Mitigation Scheme	Mitigation Strength	Board Layout Complexity	Ease in Meeting Timing Constraints	Power Consumption	Component Cost
No mitigation (power cycling)	Weak	Low	Normal	Typical	Low
XTMR	Medium	High	Reduced	~3X typical	Low
Configuration management (scrubbing)	Medium	Low	Normal	Typical	Medium
XTMR + Configuration management	Strong	High	Reduced	~3X Typical	Medium
Redundant devices + configuration management	Strongest	Medium	Normal	2–4X typical	High

Source: Brendan Bridgford, Carl Carmichael, and Chen Wei Tseng, "Single-Event Upset Mitigation Selection Guide", XAPP987 (v1.0) March 18, 2008

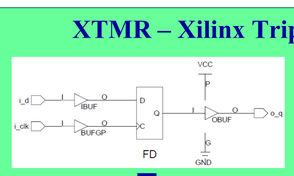
MDT CSM FPGA, run time ~ O(10h)



Source: Brendan Bridgford, Carl Carmichael, and Chen Wei Tseng, "Single-Event Upset Mitigation Selection Guide", XAPP987 (v1.0) March 18, 2008

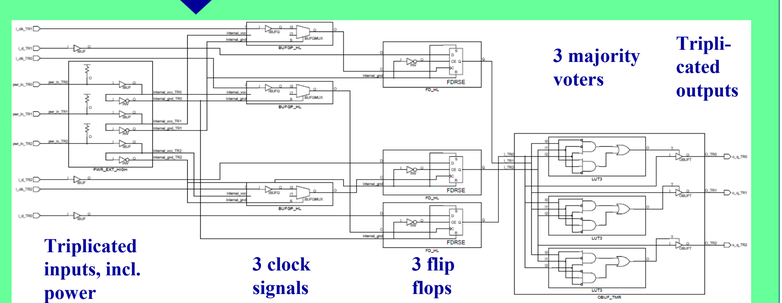
Feasible for the Xilinx Virtex-II FPGA on the CSM Board
- Apply Xilinx Triple Module Redundancy (XTMR)
- Use of failsafe FSM to avoid lock-ups
- Configuration memory scrubbing using a self-hosted scrubbing unit to prevent accumulation of SEUs that would lead to malfunction even if TMR is used.
- Check CSM status via slow control regularly during runs. Reprogram the FPGA and reload the user settings if an error is detected.
- Power-cycle the CSM during every run break or at least reboot the FPGA.

XTMR – Xilinx Triple Module Redundancy

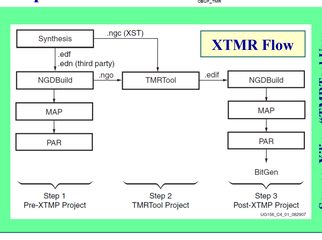


Schematic of single flip flop before and after application of XTMR.

Xilinx TMRTool Software

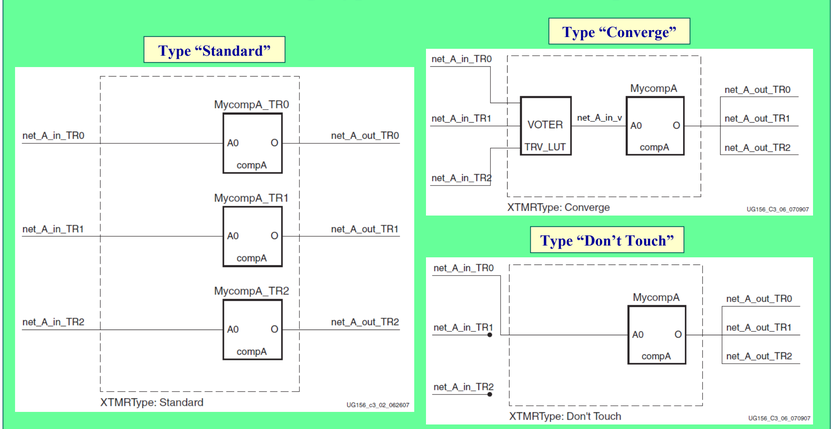


XTMR Features
- Software from Xilinx (TMRTool) for Windows
- Extra step in firmware design flow
- Quite easy to use: almost push-button solution
- Automatic triplication of design parts
- Removal of half-latches (weak keeper)
- Replacement of critical blocks (e.g. SRL16)
- Option to leave out parts from triplication



Source: Xilinx, "TMRTool User Guide", UG156 (v2.2) September 12, 2007

XTMR – Setting Types for Individual Components



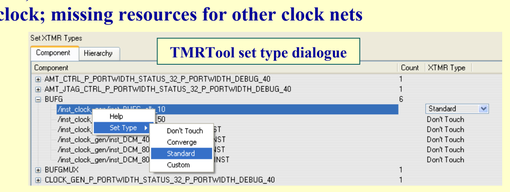
After synthesis, the EDIF file can be opened in TMRTool. The logic blocks are shown in a tree-like structure. From there, the user can select 4 different types how each component is treated by TMRTool:
- Standard: The IOs and the logic function of the block are triplicated.
- Custom: The user must provide a custom model with triplicated IOs and adequate function.
- Converge: The component is not triplicated. If an input signal comes from a triplicated net, a voter is inserted before this input. The output signals are faned out to 3 nets.
- Don't Touch: The component is not triplicated. If an input signal comes from a triplicate nets only the "TR0" net is connected to the input. No voter is inserted before the input.

Application of XTMR on CSM Firmware

Limitations for CSM firmare
- No triplication of IO-pins possible, because not foreseen in PCB design
- Only a part of the logic can be TMR'd due to limited FPGA resources (global clock nets, RAMs, logic elements)
- Only the main clock for device access via slow control can be triplicated. The remaining 4 clock nets for data processing cannot be triplicated.
- No use of external power (GND or VCC) possible, unless modifications to PCB are made.
- Timing critic nets which need register placement in IOBs cannot be triplicated.

Critical parts of CSM Firmware are triplicated using the TMRTool software
- Triplication of complete Control Part: interfaces to
  - JTAG (slow control)
  - TTCRX (clock and trigger receiver chip)
  - GOL (high speed serializer ASIC) interface
- Triplication of main (10 MHz) clock; missing resources for other clock nets
- Parts of data path TMR'd:
  - input stage
  - flow control
- Parts of data path not TMR'd:
  - serial to parallel converter
  - input data FIFOs

TMRTool set type dialogue



Setting up XTMR for CSM firmware
1. Set "Power Source" to "Internal". This is necessary unless an external reference power source on the PCB is available.
2. Apply the XTMR type "Standard" to all components.
3. Remove components that should not be TMR'd, e.g. IOs, clock nets, parts of data path
   - whenever possible, use the type "Converge" to benefit from upstream triplication
   - some components need to be set to "Don't Touch", e.g. LVDS IOs, DCMs

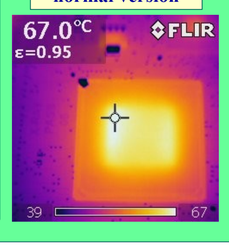
Effects of XTMR Applied on CSM Firmware

- TMR design flow works well
- FPGA slice (primitive logic elements) usage is over 90 % with XTMR
- Issue: Increased power consumption

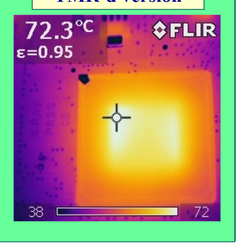
Excerpt of place & route report.	normal version	TMR'd version
Number of BUFGMUXs	7 out of 16 43%	9 out of 16 56%
Number of DCMs	2 out of 8 25%	2 out of 8 25%
Number of External DIFFMs	73 out of 228 32%	73 out of 228 32%
Number of LOCed DIFFMs	73 out of 73 100%	73 out of 73 100%
Number of External DIFFSs	73 out of 228 32%	73 out of 228 32%
Number of LOCed DIFFSs	73 out of 73 100%	73 out of 73 100%
Number of External IOBs	253 out of 456 55%	255 out of 456 55%
Number of LOCed IOBs	253 out of 253 100%	255 out of 255 100%
Number of RAMB16s	19 out of 56 33%	19 out of 56 33%
Number of SLICEs	4480 out of 10752 41%	9986 out of 10752 92%
Number of TBUFs	0 out of 5376 0%	6 out of 5376 1%

Increased power consumption results in higher component temperature
- FPGA: Increased core current by 0.2 A, additional 0.3 W dissipation
  => Increase in temperature of ~ 5°C
- Voltage regulator for FPGA core voltage (1.5V): additional 0.5 W
  => Increase in temperature of ~ 21°C
- Mounting of heat sinks on affected components is reasonable

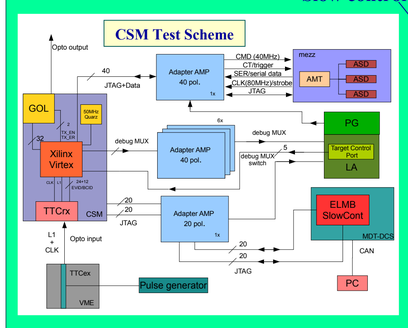
normal version



TMR'd version



Testing of CSM Firmware



Slow control
Logic analyzer
Logic analyzer pods

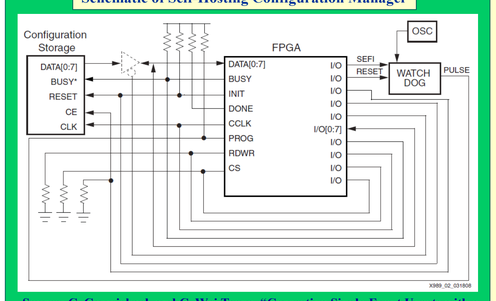
CSM board with Xilinx FPGA
Adapter boards

Test procedures and performance results of TMR'd firmware
- Verify new firmware against "golden reference" in simulation and on real system
- Test in the laboratory with pattern generator and logic analyzer
- Test in the laboratory with 3 AMTs and FILAR card (25 and 50 MHz GOL speed)
- Stimulate AMT with pulse generator
- Test at cosmic ray test setup of the LMU in Garching with 18 AMTs, i.e. a full MDT chamber
  -> TMR'd CSM sitting in test setup since Nov 2009
  -> Measurement of drift spectra shows no difference
  -> One hook-up observed during operation of several days, reason possibly other than firmware (software, slow control etc.)

=> All tests show normal operation.
=> No issues with timing or routing resources.

CSM Future Plans

Schematic of Self-Hosting Configuration Manager



Source: C. Carmichael, and C. Wei Tseng, "Correcting Single-Event Upsets with a Self-Hosting Configuration Management Core", XAPP989 (v1.0) April 2, 2008

Configuration memory scrubbing
- Due to PCB-Layout, only self-hosted configuration memory scrubber possible for CSM
- Improves radiation tolerance

Choice of implementation
- FSM: most robust solution, but consumes a lot of FPGA resources; limited complexity in scrubbing algorithm
- Soft-Processor (Picoblaze): small footprint, flexible, powerful, but memory is vulnerable to SEUs

Current CSM board
- Implementation of self-hosted scrubber to heal configuration memory SEUs
- Tests with arbitrary configuration bit errors injected into FPGA via JTAG
- Tests of CSM firmware under radiation in test setup and finally at ATLAS
  - normal version
  - TMR'd version
  - TMR'd version + configuration memory scrubbing

New version of CSM board for ATLAS upgrade
- Replace slow control and readout link with new system (GBT)
- Replace FPGA with respect to higher radiation environment
  => Virtex-5 offers better solution for SEU correction in configuration memory
  => Alternative: Switch to flash-based FPGAs like ProASIC3 from Actel
- Implement front-end trigger and selective readout: new feature to reduce data volume