Performance of a New Preamplifier-Shaper-Discriminator Chip for the ATLAS MDT Chambers in 130 nm IBM Technology

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The SLHC project at CERN foresees an increase of the peak luminosity of the LHC by a factor of up to 10 beyond the nominal value of 10^{34} cm^{-2} s^{-1}. The corresponding hit rates in the MDT chambers of the ATLAS Muon Spectrometer, mainly due to converted gammas and neutrons from cavern background, will lead to data rates in excess of the presently available readout bandwidth and high radiation damage, calling for at least partial replacement of the readout electronics. For the front-end ASD we selected the IBM 130 nm CMOS 8RF-DM technology because of its accessibility via CERN and also in view of possible synergy with the front-end chip development for the ATLAS Inner Detector.

Each of the 4 channels of the ASD chip contains a preamplifier, a three-stage shaper and a discriminator with lvds-output. One of the four channels has an analogue output to monitor the pulse shape before the discriminator. The chip is mounted on a 2-layer PCB and connected to an input protective network of identical design to the present system. To avoid possible interference, no digital circuitry was implemented on the chip at this development stage, the discriminator threshold being supplied from outside. In the chip layout, the low-resistive E1 and L1 layers of the 8RF-DM architecture were used for optimum on-chip grounding and supply voltage distribution.

Results with test pulses show good agreement with the performance of the existing amplifier as well as with simulation. Gain uniformity between the 4 channels inside a chip and between different chips is within 2%, cross-talk below 1.5%. Noise corresponds to 6000 electrons (RMS) at 10 pF external capacitance, typical for the MDT readout. All measurements were done at the nominal supply voltage of 3.3 V, resulting in a power consumption of 24 mW per channel. We discuss the next development steps, i.e. addition of a Wilkinson ADC for each channel, implementation of a DAC for programmable on-chip threshold generation, on-chip test pulse circuitry and addition of JTAG controls. As the pulse height is proportional to the supply voltage, on-chip LDO voltage regulation will also be implemented. Results from neutron irradiation are still under evaluation.